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Signal Detection of Multi-Channel Capillary Electrophoresis Chip Based on CCD

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A kind of multi-channel capillary electrophoresis (CE) chip signal detection system based on CCD was developed. The output signal of the CCD sensor was processed by a series of pre-processing circuits and ADC, and then it was collected by the Field Programmable Gate Array (FPGA) chip which communicated with a host computer. The core in FPGA was designed to control the signal flow of the CCD and transfer the data to PC based on a Nios II embedded soft-processor. The application of PC was used to store the data and demonstrate the curve. The measurement of the fluorescent signals for different concentration Rhodamine B dyes is presented and the comparison with other detection systems is also discussed.

Keywords: Capillary electrophoresis, Multi-Channel, CCD, SOPC

1. INTRODUCTION

LAB ON A CHIP technology has been rapidly developing in recent years. Most instruments can be incorporated into a small chip achieving sample pretreatment and analysis [1-4]. Among many kinds of lab on chip, the capillary electrophoresis (CE) chip has progressed greatly since its introduction many years ago. This technique offers short analysis times, small sample, electrolyte consumption, and low waste generation, which was widely used in genome sequencing project, epidemic disease testing and drug screening. Up to now the CE chip system has attracted more attention for researchers not only in the clinical analysis but also in the forensic sciences, even in the search for extraterrestrial life [5-7]. The increase in experimental complexity demands more samples to be analyzed and thus some high-throughput technologies have been designed, like the multi-channel CE chip system [8-11].

In these systems, many sample detection methods such as electrical, chemical, and optical techniques were developed, [12]. Over these approaches, the fluorescence technique of optical detection approach is the most promising one for the CE chip which has high stability, low detection limit and good discrimination capability advantages [13]. However, the conventional optical structure of the confocal detection system is complicated and larger in size, which limits the miniaturization and integration of CE chip system. Thus, a high-throughput, simply controlled fluorescence detection instrument with less optical components should be developed.

A multi-channel capillary electrophoresis with laser induced fluorescence detection system based on CCD is presented in this paper. To realize the system, the FPGA chip with Nios II embedded soft-processors is utilized. Because the FPGA-based systems combine the advantages of digital signal processors (DSPs) and Application Specific Integrated Circuits (ASICs), they include shorter design time, reusability, low cost, less human resource requirements, increasing system safety and they are easy to upgrade [14-15]; the soft-processor is the inherent flexibility that allows specialization to an application through configuration and provides access beyond the actual FPGA chip through integrated standard or custom interfaces[16]. In this work, the output signals of CCD were processed by a series of pre-processing circuits and A/D chip, then the signal was collected by the FPGA board with the core of an embedded Nios II software processor and transferred to a host computer [17]. There were two software parts for the detection system. One was the soft core in FPGA, which was designed to receive the signal of the CCD and send the data to PC. The other one was an application on host based on Visual C++, which was used to process and show the detection result.

2. STRUCTURE OF THE DETECTION SYSTEM

A typical experimental detection system for the CE chip with the CCD image sensor is shown in Fig.1. The beam from the semiconductor laser was positioned in the micro channel. The sample was driven by the high-voltage power through the detection point, then the fluorescence was excited and captured by the CCD. The signal data from the CCD was pre-processed by the FPGA board and received by the host computer.

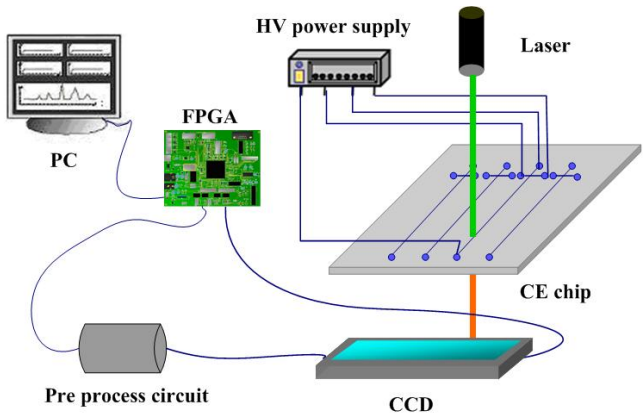


Fig.1. Structure diagram of the detection system

FPGA chip was the main logic controller and it generated the driving timing pulse for the CCD and trigger signal for the A/D converter. The analog signal from the CCD sensor through the differential, filter and amplifier circuits was sent to the A/D chip TLC5510. The digital pixel-signal was processed by the embedded Nios II processor and transferred from the hardware board to the host computer via RS232. The hardware architecture is shown in Fig.2.

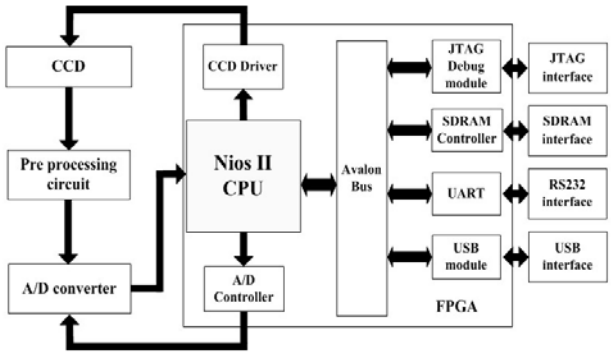


Fig.2. The architecture of the basic hardware

2.1. CCD driver module

TCD1208AP fabricated by TOSHIBA Company was selected as the CCD sensor, which is a high sensitive and low dark current 2160-element image device. The image sensing element size is 14μm by 14μm, the over length is 30.2mm. The microfluidic channel width of the capillary electrophoresis chip is 100μm and the distance between the two micro channels is 6mm, so the sensor element size is large enough for the CE chip detecting.

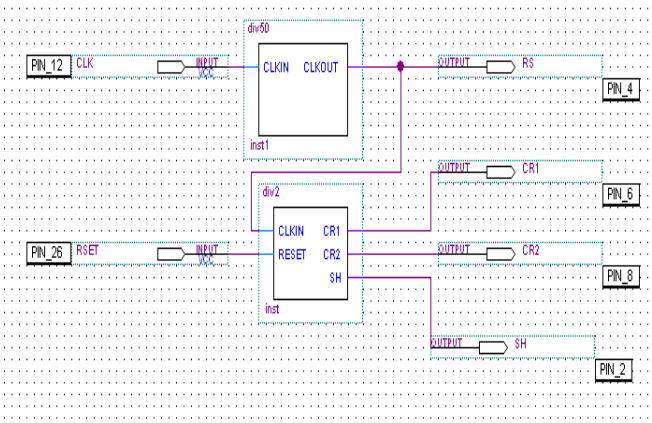


Fig.3. The schematic of CCD driver

The driver module of the FPGA chip generated the clock time for CCD by the time sequence which was designed with schematic composer as shown in Fig.3. The pulse of light integral SH with the charge transfer pulse CR1 and CR2 was set up by the software in the counter mode. The clock cycles could be adjusted by the counter according to the CCD drivers. The input clocks determined all the output pulse, but they were mutually independent, actually avoiding the race and hazard between RS and SH.

The clock frequency of signal CLK was 50MHz and the working frequency of CCD was 1MHz, therefore the module Div50 divided the CLK by 50 and generated the reset signal RS with duty ratio 1:3. The module Div2 divided the RS by 2 that produced the two phase pulse CR1 and CR2. Their frequency was 0.5MHz, and the duty ratio was 1:1. The SH controlled the output signal frequency of the CCD. The simulation waveform is shown in Fig.4. As can be seen, the width of the wide pulse of the CR1 and CR2 is larger than the SH signal pulse where the pulse number is more than 1106 in one cycle.

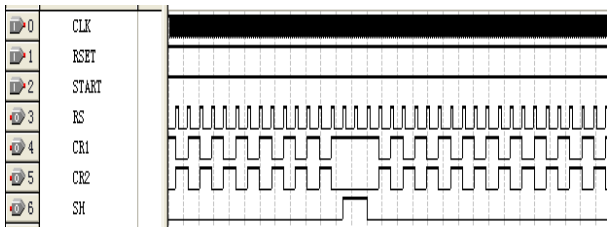
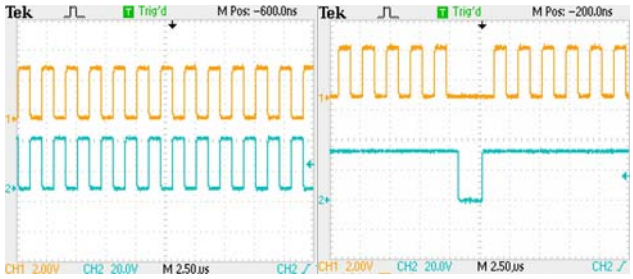


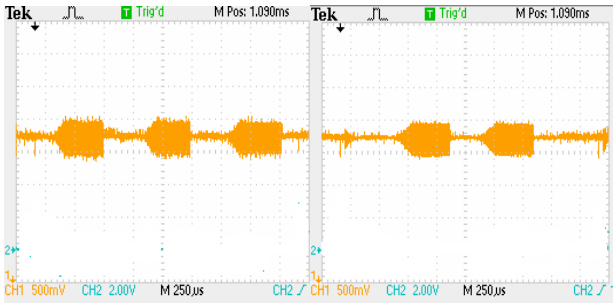
Fig.4. Simulation waveform of CCD driver

After the device configuration, the code was compiled and downloaded into the FPGA chip under the Quartus II development environment. The output waveform of the pins is shown in Fig.5 by the DSO (Digitizing Storage Oscilloscope), the waves meet the phase and amplitude requirements of the CCD device. Using the 532nm laser as the light source, the CCD covered with a black film having some slits was used to test its ability. The waveform detected by CCD, as shown in Fig.6, demonstrated that the TCD1208AP chip is performing normally under the control of CCD driver module.



(a)Charge transfer pulse CR1,CR2 (b) The pulse of SH and CR1

Fig.5. Driving Waveform on DSO



(a) The film with 2 slits (b) The film with 3 slits

Fig.6. Signals on DSO with different slits

2.2. Differential circuit

TCD1208AP CCD has two outputs which are the signal output (OS) and the compensation output (DOS). In the original output signal, the effective signal of OS is only several hundred mill volts and there are many pulse disturbances caused by the reset signal. Thus, the AD620 amplifier was selected to eliminate the useless signal and amplify the effective signal by the differential amplification circuit. The OS and DOS were separately connected to the reverse phase and same phase inputs of the AD620.

2.3. Filter and amplifier circuit

In the fluorescence detection, the output signal of the CCD device was always imposed with high-frequency noise, so a low-pass filter was used to get the accurate value. The circuit diagram for the voltage-controlled voltage source (VCVS) low-pass filter unit is shown in Fig.7.

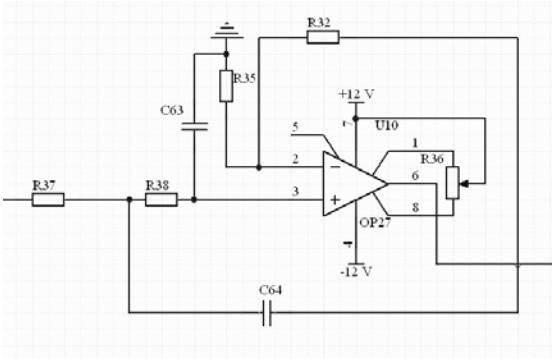


Fig.7. Circuit diagram of VCVS second-order low-pass filter

It was composed of RC filters and a proportional OP27 amplifier. According to the VCVS second order low-pass filter, the cutoff frequency is

$$f_o = \frac{1}{2\pi\sqrt{R_{37}R_{38}C_{63}C_{64}}} \tag{1}$$

Based on the Nyquist sampling theory, the cutoff frequency was adjusted. While it was the same with the frequency of the reset pulse, the noise could be reduced more, the parameters were designed as C63 = C64 =100pF, R37=R38=1.6kΩ. The differential circuits only amplify the current of the signal and suppress the interference, which do not increase voltage amplitude more, so the output signal is still small. Therefore a voltage amplifier circuit was designed to process the signal before it was sent to the A/D converter.

2.4. A/D conversion

To realize high speed sampling, a Texas Instruments (TI) TLC5510 was chosen as the analog digital converter which is a CMOS, 8-bit, 20MSPS analog-to-digital converter (ADCs) utilizing a semi-flash architecture [18]. It includes internal-reference resistors, a sample-and-hold circuit, and parallel outputs with high-impedance mode, which greatly simplifies the design of the external circuit. Driving pulse CLK for A/D converter is generated by the FPGA chip. The light integral SH of CCD pulse controls the OE of the ADC to achieve the signal output, and synchronizes the digitizing process.

3. SOFTWARE ARCHITECTURE

3.1. Embedded system design

The CCD detection system is based on a FPGA chip which is designed as a system-on-a-programmable-chip (SOPC) with the embedded Nios II software processor. Depending on SOPC technology, the detection systems should be more compact and high performance. The Nios II application is used to control signal processing and data streaming. The whole system was designed in SOPC builder of Quartus II development environment. The main unit consists of a Nios II processor, on-chip memory (RAM and ROM), peripheral interfaces, I/O logic control, data converters and some Avalon slave components which are mapped to Avalon bus. Meanwhile, its respective address and interrupt requirement sequence number were generated automatically. The PLLs for Nios II and the memory clocking were the only additional components [19].

The main systematic task undertaken by the Nios II was to accomplish the control of the CCD and A/D converter. The host PC sent the "Begin" command to the FPGA board, the Nios II soft core started the CCD driver with A/D conversion module and received digital pixel signal. Each frame of the signal received by the FPGA chip was loaded into SDRAM memory buffer. When one frame completed, the data was sent to the host computer, the procedure continued to capture the next frame until the signal collection closed; the process is depicted in Fig.8. This program was written in C and downloaded to the FPGA board by Alter's Nios II IDE [20].

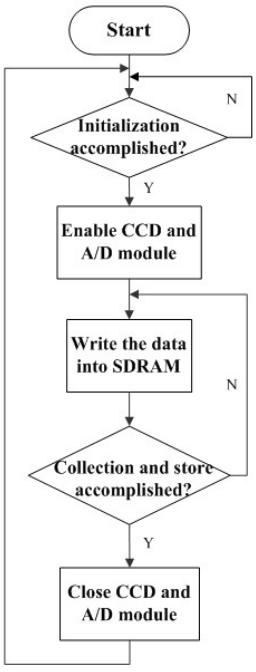


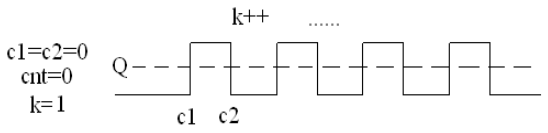
Fig.8. The flow diagram of program executed in Nios II

3.2. *Host Applications*

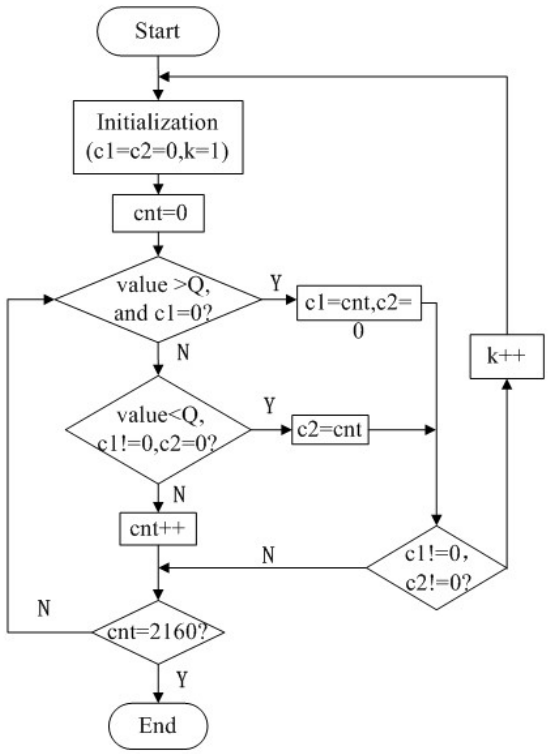
The application frame was designed by App Wizard of the VC++, and utilized the MFC program to complete it. This data acquisition software provided a friendly man-machine interactive interface and realized some functions such as data accept, signal processing, display and data store.

The CCD data from the FPGA board was put into the two dimensional arrays (400×2160). Each row stored one frame data, and different row corresponded to different sampling times. For drawing the graphs, the data in the array buffer need to be further processed, including D/A, channel recognition and data filter.

The channel recognition principle is shown in Fig.9. Q is the pixel reference value; c1 and c2 are the pixel numbers of the two sides of the micro channel, the pixel data between c1 and c2 are the valid signal value in this channel. The channel number is k, cnt is counter increased by one which is triggered by rising edge of RS. The program will detect all the pixel data with the increase of the cnt. When the value is higher than Q, c1 is given the current cnt number, if it is lower, c2 is given the cnt. At the initial stage, the default value of k is 1, the default channel is No.1, after both c1 and c2 have value, the k increases by 1, and turns to the next channel. Then this step is repeated until all the pixels are processed.



(a)



(b)

Fig.9. (a) The diagram of channel identification (b) The flow chart of program for channel identification

4. DISCUSSION

The multi-channel CE chip was pretreated with deionized water and the running buffer. Then Rhodamine B dyes with different concentration (1.0×10^{-5} mol/L, 1.0×10^{-4} mol/L, 1.0×10^{-3} mol/L, 1.0×10^{-2} mol/L) as the samples for the experiment were driving to the four channels, respectively, by the high voltage. [21-22]. While the sample moves to the detection point, the laser excites the fluorescence which is received by the CCD detection system.

The signal from the CCD was transmitted to the FPGA chip and through the UART-port to the windows XP based host computer. The data was processed by the application and the results could be displayed on the screen. The interface could display not only the detecting curve of single channel but also the four channel curves at the same time. The fluorescence intensities of different concentration Rhodamine B dyes were measured in the four-channel CE chip simultaneously, utilizing the CCD detection system as shown in Fig.10. From the image, the four clear peaks of the fluorescence intensities are obtained, they have sharp and low noise profile. Fig.11 shows the fluorescence intensities of four concentration Rhodamine B dyes detected in a single channel CE chip four times by past self-developed conventional fluorescence detection system. In this figure, the curve profiles are remarkably broadened and unstable; the background noise level is so high. The comparison result shows that the signal of the CCD detection system has better stability and higher signal to noise ratio than the conventional fluorescence detection system.

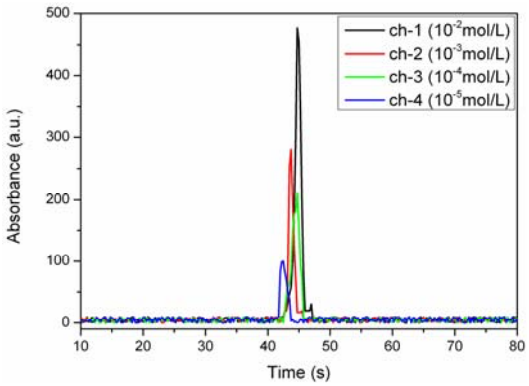


Fig.10. Fluorescence intensity vs. time (s) in CCD detection system

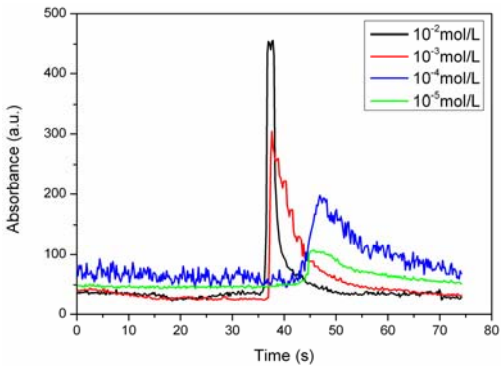


Fig.11. Fluorescence intensity vs. time (s) in conventional detection systems

5. CONCLUSIONS

The design of a multi-channel capillary electrophoresis signal detection system based on CCD and FPGA was presented in this article. The FPGA chip is configured as a System On Programmable Chip with a Nios II soft processor. The system controlled by the soft core provides more flexibility for processing and transferring of the CCD signal. The experiments demonstrate that the detection system has the advantages of high throughput, better stability and higher SNR compared with a conventional fluorescence detection system. However, this system also needs more improvement, we will continue to increase the integration of CE chip with the CCD in the semiconductor technology and measure more kinds of samples such as the amino acids, proteins and DNA to test the performance of this system. With the efforts, we strongly believe this multi-channel CE signal detection system will become a more integrated, less expensive, high throughput and powerful commercial detecting platform for the life sciences in the near future.

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