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Study of Small-signal Model of Simple CMOS Amplifier with Instability Compensation of Positive Feedback Loop

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The paper deals with precise analysis of simple AC variable gain CMOS amplifier. The circuit can be used as a simple voltage follower (6 MOS transistors are required) or amplifier. The main attention of this work is focused on a small-signal model of the proposed block and effects of additional passive network leading to compensation of its instability. The continuous gain adjusting in range from 1.1 to 10 (0.8 – 20 dB and with bandwidth 4.9 - 90 MHz at 5 pF load capacitance) is possible and the proposed amplifier is suitable for implementation in systems, where lower range of gain adjusting and large dynamical range is required. Theoretical analyses are supported by PSpice simulations (TSMC 0.18 um technological models) and experimental measurements with commercially available CMOS transistor fields (ALD1106/7) also confirm the discussed behavior of the amplifier.

Keywords: Active elements, instability compensation, variable gain amplifier, voltage buffer, voltage follower, voltage gain adjusting.

1. INTRODUCTION

MANY TYPES OF ELECTRONIC control in frame of the active device are known [1]. We can discuss methods like transconductance (g_m) control [1], [2] intrinsic current input resistance control (R_x) [1], [3] current gain control (B) [4-8], voltage gain control (A) [9], and their combinations [10-14].

Discussed methods [2], [3] may be used for construction of controllable amplifier, where such parameter can serve for electronic control of the gain. Unfortunately, control of parameters (even value of passive resistor network) that are suitable for gain change may cause problems with the stability of such circuits employing feedback loop(s). This problem is typical for very simple solutions, for example in Miller opamp [15], transconductance-based two stage amplifiers [16], or multistage systems [17].

Some types of commercially available variable gain amplifiers (VGAs) are available (VCA810, LMH6505), but their internal structures are complicated (multipliers and transconductance sections – many CMOS or bipolar elements) or they are usually hidden to designers. Digital control of gain (e.g., well-known AD603) is a typical feature for the majority of commercially available devices, which is not suitable for some of the pure analog circuits and applications where continuous control of parameter is required (control of condition of oscillation in oscillators, control in sensitive systems, etc.).

We also studied several hitherto published solutions [18-29] of the VGAs and simple CMOS amplifiers. The main attributes of these solutions are focused on wide-range gain control (± 40 dB) and they usually require many bias sources ([18], [19], [22], [23], for example). Many of the known structures are based on specific utilizations of the differential (transconductance) sections [18-23], [28], [29] but some circuits also operate without a differential section [24-27]. Moreover, many of the previously introduced structures use biasing current sources not only for biasing of the transconductance sections, for example [24], [25], [27]. The bias source of the transconductance section [18-23], [28], [29] is necessary for g_m adjusting. Of course, it causes changes of the DC current from the supply source and therefore if gain is rising, power consumption increases substantially.

We can obtain really simple solutions of such circuits by various design methods but precise investigation of stability and compensation is always required due to feedback loops in these systems as will be discussed in this work. Our paper is focused on the analysis of a simple CMOS variable gain voltage AC amplifier (shortly CMOS VGA). Our aim is to investigate a simple adjustable voltage amplifier with gain range up to several units. It is sufficient for use in AGC systems of oscillators, which require lower gains (units) for fulfillment of oscillation condition [12].

We prepared simple VGA structure consisting of P-MOS current mirror together with voltage to current converters (two N-MOS transistors), basic inverter, and feedback loop (with positive feedback) suitable for control of gain. We intend to design simple and controllable structure of the VGA allowing low range of gain control (for specific purposes), where minimal number of transistors and passive elements is required, in comparison to the above discussed types of commercially available VGAs. For example, Miller opamp [15] has some better features but, unfortunately, is also more complicated (further biasing required) than our solution. We want to show that even systems with positive feedback can operate correctly if adequate but simple

precaution (simple compensation) is implemented. In comparison to classical approach based on pure transconductance differential pair [15], this solution does not require a biasing current source.

The proposed VGA has several advantages: 1) very simple and compact solution; 2) proposed structure applicable as a voltage follower (buffer) or a controllable voltage amplifier; 3) low power consumption, low supply-voltage of CMOS solution; 4) static power consumption influenced (increased) minimally by gain control under operation with AC coupling; 5) sufficient dynamical range (± 600 mV in simulation). Circuit can also work as a simple voltage buffer without necessity of control (full feedback and only 6 transistors are sufficient). However, there are also disadvantages: 1) operation as AC single-ended amplifier only – very high value of DC component of input voltage influences cross-current balance of MOS (therefore also power consumption); 2) low power supply rejection ratio; 3) worse linearity of DC transfer characteristics if single N-MOS equivalent (in triode regime) of resistor is used for gain control. Nevertheless, circuit is more than sufficient for intended purposes. Note that the presented example of VGA, suitable for deep analysis, is quite similar to standard opamp-based solution of non-inverting amplifier with feedback network. However, used CMOS solution has different attributes (differential transconductance section with bias current tail source and the second standard emitter follower stage is not used in our case) [15].

The paper is organized as follows: Introductory section discusses reasons for necessity of simple VGA solutions and their careful analysis. Features and behavior of the VGA model are explained in section 2 together with complete theoretical ideas and important relations. Section 3 provides simulation results and investigation of stability in frequency and time domain together with preliminary demonstration of impacts of compensation network in detailed simulation with the CMOS model. Section 4 shows measurement results of proposed circuit employing commercially available CMOS transistor fields in order to prove expected behavior of basic uncompensated VGA. Both above mentioned sections form an overall view of circuit performance mainly in the frequency and time domain. Then, section 5 includes accurate small-signal models of VGA representing real behavior based on parameters extracted from detailed PSpice simulations, analyses sources of possible instability, solves this problem by additional compensation network and discusses additional impacts of compensation elements on overall performances. Section 6 presents features of simple electronic control (by DC voltage) suitable in this type of VGA. Tabular comparison and short discussion of presented structure and selected results relating to hitherto published works is placed in section 7. All important features and ideas are summarized in conclusion (section 8).

2. SIMPLE CMOS AMPLIFIER

Fig.1. shows block diagram of the one-loop feedback system. We established really simple structure for demonstration of intended features. The principle is very similar to classical transconductance amplifier [2] with voltage buffer – opamp with one difference. DC bias current source of differential pair and standard second stage (emitter follower) is not employed. The circuit in Fig.1. (CMOS solution in Fig.2.) utilizes two equal transconductance sections (g_m – two N-channel MOS), inverting amplifier ($-A$) with high gain (M_5 and M_6 create basic voltage inverter in CMOS digital logic), and voltage attenuator which is realized by passive resistive divider in the simplest case. This subcomponent arrangement allows correct operation with positive feedback. Supposed equality of both g_m-s (M_1, M_2) is achieved by W dimensions. Proposed design also supposes the existence of high impedance node (Z_k). Blocks in the feedback branch (g_m, E_g) create positive feedback of signal from output to Z_k.

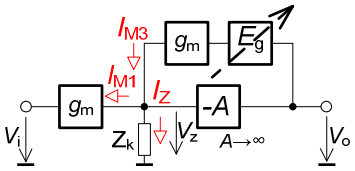


Fig.1. Behavioral block model of the CMOS VGA.

Purpose of the R_m and C_m elements shown in Fig.2. is the frequency compensation as it will be explained later in detail.

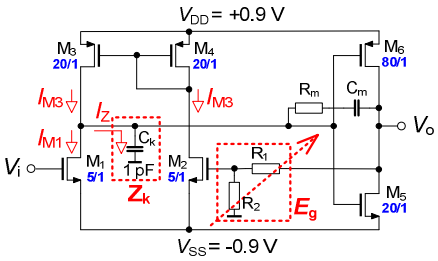


Fig.2. Proposed CMOS implementation of VGA.

We suppose perfect matching of CMOS DC parameters. The voltage V_Z across impedance Z_k is the starting point of our discussion: $V_Z = I_Z Z_k = (I_{M3} - I_{M1})Z_k$. The DC current flowing to the impedance Z_k is almost insignificant and negligible, because this node influences mainly high-frequency features. We also know that $V_Z = -V_o/A$ and the following expression can be established:

$$-\frac{V_o}{A} = \left(V_o E_g g_{mM2} - V_i g_{mM1}\right) Z_k . \tag{1}$$

We can carry out mathematical rearrangements of (1) and get:

$$\frac{V_o}{V_i} = \frac{A g_{mM1} Z_k}{A E_g g_{mM2} Z_k + 1}, \tag{2}$$

and if we suppose $Z_k \to \infty$ or $A \to \infty$ for this ideal determination only, (2) changes to:

$$\frac{V_o}{V_i} = \frac{g_{mM1}}{E_g g_{mM2}}. \quad (3)$$

Transconductances of M_1 and M_2 are equal, therefore, final expression for voltage gain is:

$$GAIN = \frac{V_o}{V_i} = \frac{1}{E_g} = 1 + \frac{R_1}{R_2}, \quad (4)$$

which is very similar to classical opamp based non-inverting amplifier with resistive divider [15]. Resistor R_2 can be replaced by electronically controllable grounded equivalent (MOS in triode regime [30]). The overall gain of the VGA is completely determined by the amplification/attenuation of the feedback loop. Utilization of simple passive attenuator allows to obtain gain equal to or higher than 1.

3. Simulation Results Including Stability Test

Proposed circuit was verified by simulations in PSpice with TSMC LO EPI 0.18 µm models [31] with both presented types of control (i.e., passive resistance control and voltage control – see section 6) with power supply $+V_{DD} = -V_{SS} = 0.9$ V, $R_1 = 1$ kΩ, load resistance $R_{load} = 1$ kΩ and capacitance $C_{load} = 5$ pF (to be shorter referred as R_1, C_1 in symbols and equations in sections 4 and 5).

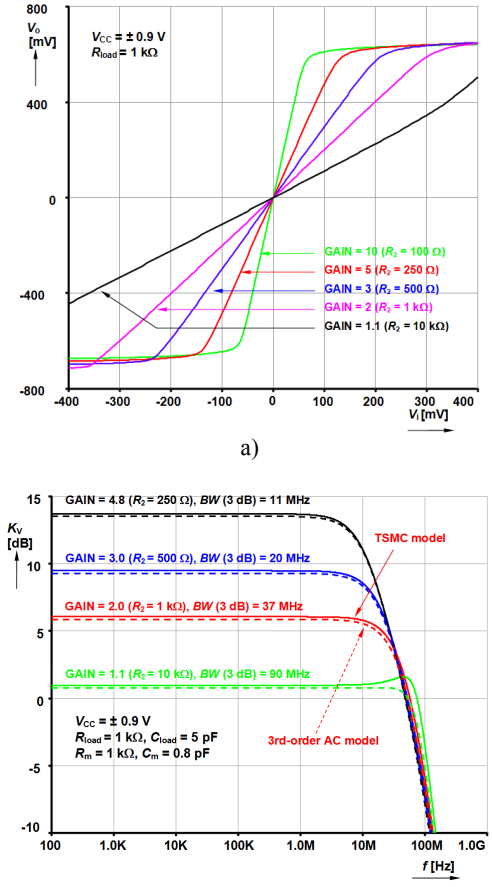


Fig.3. Transfer characteristics of VGA for different gains set by passive component (R_2 value): a) DC transfers, b) AC frequency responses.

The circuit in Fig.2. was used in simulations, where controllability of the gain by grounded resistor R_2 was performed. Resulting DC characteristic is shown in Fig.3.a). Adjusting of gain was tested from 1.1 to 10 (bandwidth 90-4.9 MHz) by change of R_2 between 10 kΩ and 100 Ω. The chosen responses in AC domain are depicted in Fig.3b.). The results of the simulation (Fig.3b.)) are compared with expected magnitude responses from AC model presented later in Fig.14. and with transfer function (8). Potential issues with stability are typical for lower gains. However, compensation resistor and capacitor in Fig.2. (C_m - tenths of pF) help to avoid any stability problems. Nevertheless, the lower bandwidth is the cost of such compensation.

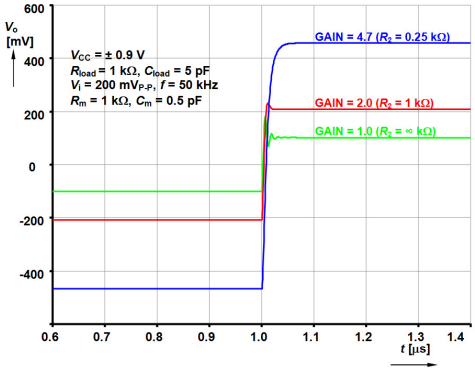


Fig.4. Detail of transient output responses for different gains when input signal is applied (its parameters are included in the figure).

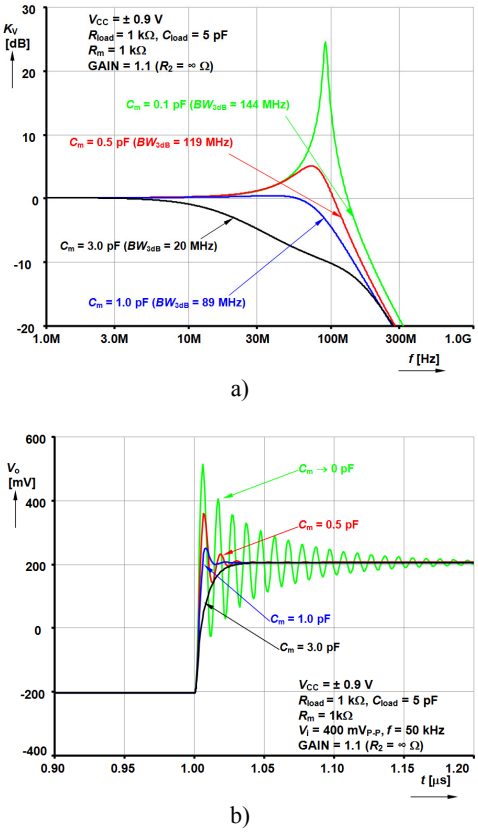


Fig.5. Influence of compensation capacitor C_m on: a) frequency response, b) transient response (gain = 1).

Simulation results were provided also in the time domain to investigate the stability of the VGA. The output transient responses of the VGA from Fig.2. for square wave excitation (V_i = 200 mV_{P-P}, f = 500 kHz) are shown in Fig.4. for different gains. Possible stability problems occur at lower gains near to 1. This issue could be solved by R_m, C_m in Fig.2. Detailed explanation will be provided in section 5. Compensation for gain equal to 1 ($R_2 \rightarrow \infty$) by different values of C_m (0.1, 0.5, 1 and 3 pF) is documented in Fig.5. Increasing C_m causes decreasing bandwidth from 144 to 20 MHz for discussed C_m changes. Detailed analysis of small-signal model of the VGA, determination of the poles, and possible problems are discussed in section 5.

4. Measurement Results

Commercially available CMOS transistor fields (Advanced Linear Devices) ALD1106 (N-MOS type) [32] and ALD1107 (P-MOS type) [33] have been used for experimental verification of the proposed VGA (Fig.2.) to confirm expected problems with stability at lower gain values and their solution. This implementation is very useful for verification of simple CMOS systems without expensive prototype fabrication (that is not necessary at this stage of our research). It provided interesting results as is described in further text. Unfortunately, parameters such as high-frequency operation and high DC accuracy are not available in this case of discrete devices. Due to this fact and $C_k \approx 6$ pF + influence of printed circuit board (PCB) the measured VGA works with lower bandwidth (-3 dB) than circuit that was simulated with 0.18 µm CMOS models. Such value of C_k is caused by input-gate capacitance (≈ 3 pF) of the transistors [32], [33]. Real loading capacitance of several units of pF (PCB and input of used voltage buffer for impedance matching) is also supposed. Despite lower bandwidth, behavior of the measured VGA in frequency and time domain is almost identical to the simulated TSMC based VGA model. Behavior of the measured circuit model of the structure in Fig.2. was tested in time, AC, DC domain, THD and power consumption are also included. Supply voltage was set to ±1.5 V. All measurements were carried out for load resistance R_L = 1 kΩ (and matched by external voltage buffer to 50 Ω for input of network/spectrum analyzer E5071C). Compensation capacitor C_m was not used in measurements. The DC and AC performances are shown in Fig.6.

Adjustability of the gain was tested in range from 1.15 to 7.04 when R_2 had five discrete values (10 kΩ, 1 kΩ, 0.5 kΩ, 0.25 kΩ, 0.1 kΩ). Only four chosen gains are presented in Fig.6. for better readability. As we can see, the experiment confirms that the control of gain (block E_g) really influences stability of the circuit, see trace for gain 1.15. Stability of the circuit is problematic mainly for lower gains around 1 as we can see from Fig.6.b) and Fig.7.a). In Fig.7., the details of transient response for low and higher gain for square wave (blue color) input testing signal (100 mV_{P-P}, 1 kHz) are illustrated.

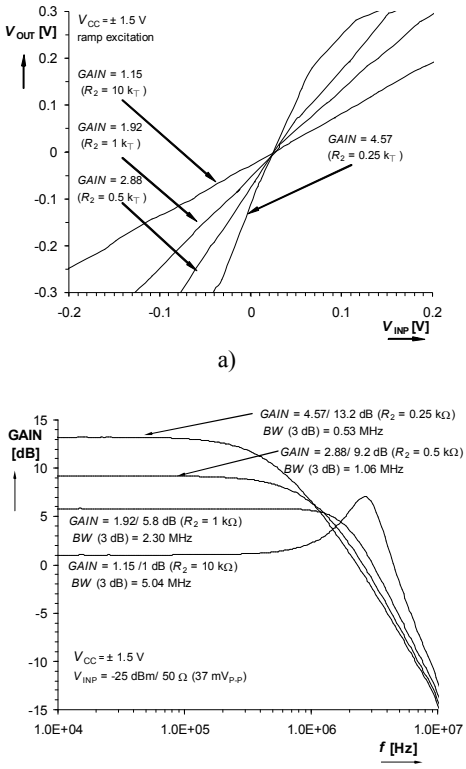


Fig.6. Measured transfer characteristics of VGA for different gains set by R_2 value: a) DC transfers, b) AC frequency responses.

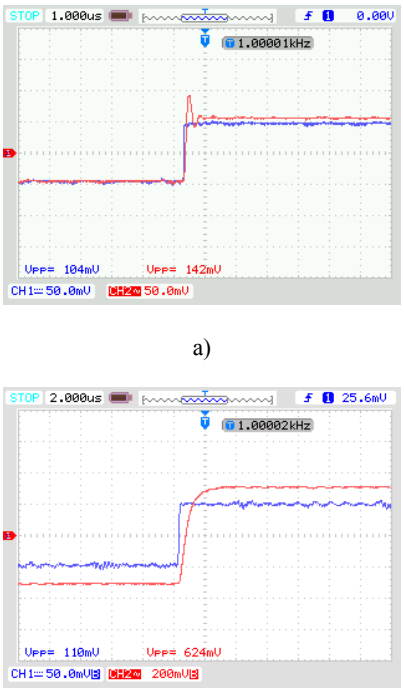


Fig.7. Stability tests of the proposed VGA (blue color - input signal, red color - output signal): a) gain almost equal to 1, b) higher gain.

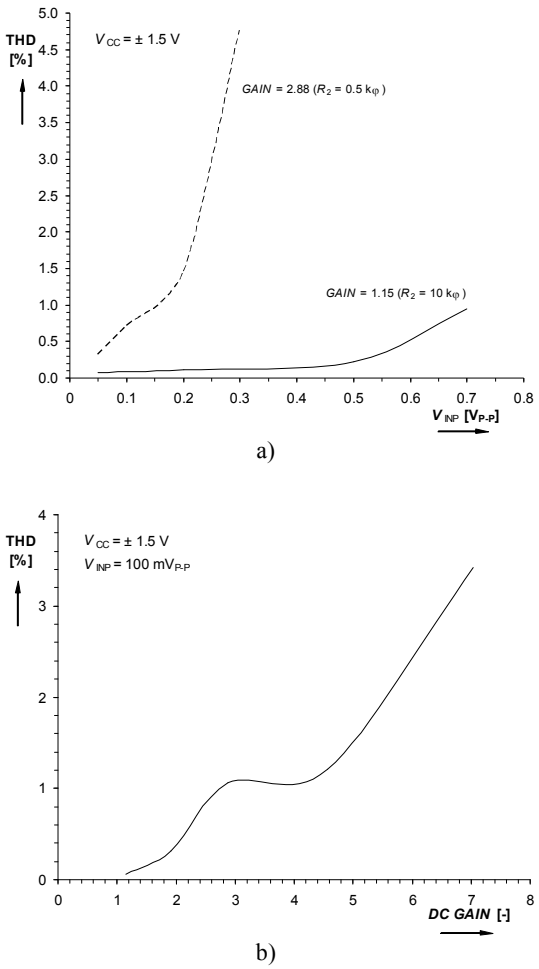


Fig.8. Measured dependence of THD on: a) input level, b) actual gain.

Following analysis (Fig.8.) presents dependences of total harmonic distortion (THD) on input level (V_{INP} was changed from 50 to 700 mV_{P-P} (1 kHz) for two different gains equal to 1 and 3) and also dependence on actual gain setting. Measured circuit works well with input levels limited to several tens of mV (maximal allowable range for acceptable THD ≤ 1 % is limited approximately to the value 100 mV_{P-P} for higher gains up to 5). An example of the spectrum for 50 mV_{P-P} and 200 mV_{P-P} input signal (when gain is equal to 2.88) is shown in Fig.9.

Power consumption of proposed VGA is documented in Fig.10. Dependence of the power consumption on actual value of voltage gain is almost constant and is below 2 mW in the whole tested range, which is really satisfactory for discrete implementation. Control of gain by standard bias current control means substantially higher power consumption and consumption is dependent on actual gain. Proper values of R_1 (together with current value of R_2) and R_{load} (1 kΩ) ensure that output current does not exceed substantial value for all values of R_2, causing rapid increase of the power consumption. For example, single voltage buffer (formed from opamp OPA2650) used for impedance matching had power consumption about 60 mW.

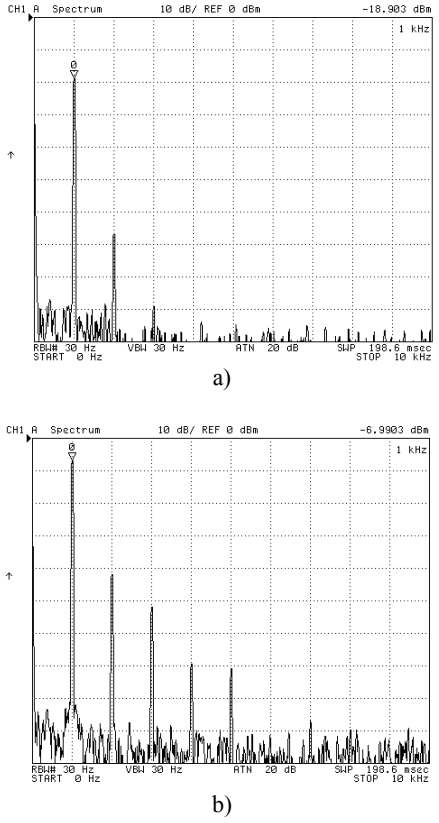


Fig.9. Measured spectrum of output response (gain equal to 2.88): a) V_{INP} = 50 mV_{P-P}, b) V_{INP} = 200 mV_{P-P}.

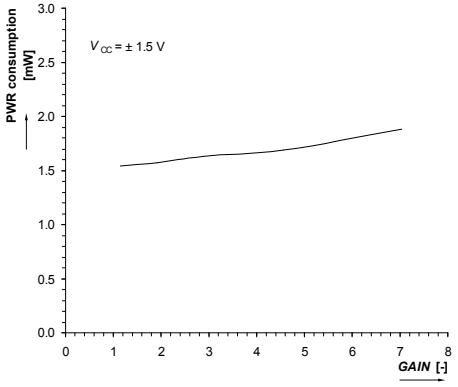


Fig.10. Measured power consumption of VGA in dependence on particular gain value.

5. AC Model of VGA and Compensation of Real System

The VGA was analyzed symbolically to reveal and to solve important influences causing possible problems with stability and bandwidth. Small-signal AC model of the VGA with the important passive and active (voltage controlled current sources and voltage controlled voltage source) elements is shown in Fig.11. Following discussion supposes that frequency features of $g_{mM1,2}$ and A do not influence the investigated frequency band. The inverting amplifier A, formed by M_5 and M_6, has gain given by $A = (g_{m5} + g_{m6}).(r_{o5} \| r_{o6})$, where $r_{o5,6}$ are output resistances of

transistors. It is obvious that real gain A is not infinite but it is sufficiently high due to the large size of the transistors.

We established and got following parameters for typical situation (based on simulation - extraction from model employing TSMC technology and estimations, some parameters were intentionally more critical than is expected): $C_{\mathrm{load}} = 5$ pF, $C_{\mathrm{k}} = 1$ pF, $R_{\mathrm{k}} = 89$ kΩ, $R_{\mathrm{l}} = 1$ kΩ, $R_{\mathrm{o}} = 16.3$ kΩ, $A = 60$, $g_{\mathrm{mM1,2}} = 530$ μS. Transfer function of the simple VGA model in Fig.11. has the form:

$$K_{VGA\_AC1}(s) = \frac{\frac{g_{mM1}A}{R_oC_lC_k}}{s^2 + s\frac{R_lR_kC_k + R_oR_kC_k + R_lR_oC_l}{R_lR_oR_kC_lC_k} + \frac{g_{mM2}AE_gR_lR_k + R_l + R_o}{R_lR_oR_kC_lC_k}}. \quad (5)$$

The frequency of the complex conjugated (dominant) poles is given by:

$$\omega_{p1} = \sqrt{\frac{g_{mM2}AE_gR_lR_k + R_l + R_o}{R_lR_oR_kC_lC_k}}, \quad (6)$$

and quality factor of the pole has the form:

$$Q_{p1} = \frac{\sqrt{\left(g_{mM2}AE_gR_lR_k + R_l + R_o\right)\left(R_lR_oR_kC_lC_k\right)}}{R_lR_kC_k + R_oR_kC_k + R_lR_oC_l}. \quad (7)$$

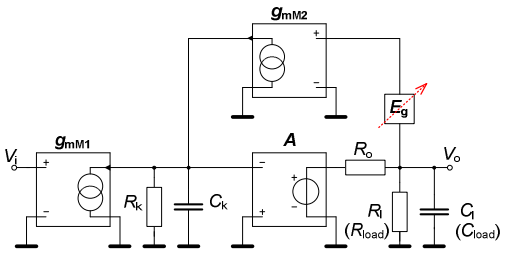


Fig.11. AC small-signal model of proposed VGA including the most important real-device effects.

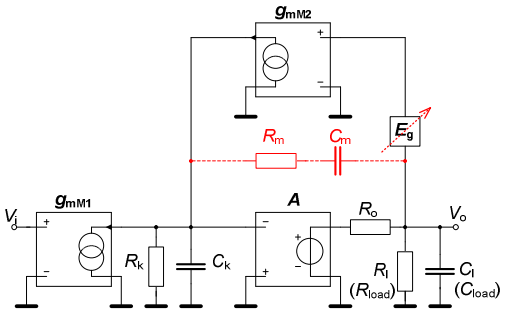


Fig.12. Compensation of the VGA by additional R_{m}, C_{m}.

Resonant peak caused by complex conjugate pole can be the source of potential instability. Therefore, we have to compensate it. One possible way how to do it is shown in Fig.12., where compensating network R_{m}, C_{m} was added. Transfer function has the character of the 3rd order low-pass filter with one zero:

$$K_{VGA\_AC2}(s) = \frac{g_{mM1}R_kR_l\left[A + sC_m\left(AR_m - R_o\right)\right]}{b_3s^3 + b_2s^2 + b_1s + b_0}, \quad (8)$$

Where

$$b_0 = g_{mM2}E_gAR_kR_l + R_l + R_0, \quad (9)$$

$$b_1 = g_{mM2}E_gR_kR_lC_m\left(AR_m + R_0\right) + R_kR_l\left(C_k + C_m + AC_m\right) + \\ + R_0\left(R_lC_m + R_lC_l + R_mC_m + R_kC_m + R_kC_k\right) + R_lR_mC_m, \quad (10)$$

$$b_2 = R_kR_lC_m\left(R_oC_l + R_mC_k + R_oC_k\right) + \\ + R_oR_mC_m\left(R_lC_l + R_kC_k\right) + R_kR_lR_oC_lC_k, \quad (11)$$

$$b_3 = R_kR_lR_oR_mC_lC_kC_m. \quad (12)$$

Overall transfer function (8) is complicated (3rd-order denominator with large expressions at the polynomial coefficients). The first approximated transfer function (approx1) of the VGA model in Fig.12. has the form:

$$K_{VGA\_AC2}^{approx1}(s) \cong \frac{\frac{g_{mM1}\left(A - sC_mR_o\right)}{R_o\left(C_lC_k + C_lC_m + C_kC_m\right)}}{\left(s^2 + s\frac{R_lC_m + R_oC_k + R_oC_m + R_lC_k + AR_lC_m + g_{mM2}E_gR_lR_oC_m}{R_lR_o\left(C_lC_k + C_lC_m + C_kC_m\right)} + \frac{g_{mM2}E_gA}{R_o\left(C_lC_k + C_lC_m + C_kC_m\right)}\right)}, \quad (13)$$

Where

$$\omega_{p1}^{approx1} \cong \sqrt{\frac{g_{mM2}E_gA}{R_o\left(C_lC_k + C_lC_m + C_kC_m\right)}}, \quad (14)$$

and

$$Q_{p1}^{approx1} \cong \frac{\sqrt{g_{mM2}E_gAR_lR_o\left(C_lC_k + C_lC_m + C_kC_m\right)}}{R_lC_m + R_oC_k + R_oC_m + R_lC_k + AR_lC_m + g_{mM2}E_gR_lR_oC_m}. \quad (15)$$

Unfortunately, this model contains right-half-plane zero given by $A/\mathrm{s}CR_{\mathrm{m}}$. This zero should be at higher frequency with respect to the first dominant pole ω_{p1} (far from ω_{p1}). We can achieve it by a larger gain A of the voltage inverter stage (M_5, M_6) than the gain of the section with M_1 to M_4.

We can also use second type of available approximation (approx2) which leads to the following transfer function, without zero:

$$K_{VGA\_AC2}^{approx2}(s) \cong \frac{\frac{g_{mM1}A}{R_oC_l\left(C_k + C_m\right)}}{s^2 + s\frac{AR_lC_m + R_o\left(C_k + C_m\right)}{R_lR_oC_l\left(C_k + C_m\right)} + \frac{g_{mM2}E_gA}{R_oC_l\left(C_k + C_m\right)}}, \quad (16)$$

$$\omega_{p1}^{approx2} \cong \sqrt{\frac{g_{mM2}E_gA}{R_oC_l\left(C_k + C_m\right)}}, \quad (17)$$

$$Q_{p1}^{approx2} \cong \frac{\sqrt{g_{mM2}E_gAR_lR_oC_l\left(C_k + C_m\right)}}{AR_lC_m + R_o\left(C_k + C_m\right)}. \quad (18)$$

Fig.13. shows an example of operation with adjustable gain E_g in magnitude response. It is clearly seen that E_g has impact on pole quality and frequency and decreases with higher gains. Both obtained transfers (13) and (16) are compared with (8) and "uncompensated" transfer (5) in Fig.13. for $C_m = 0$ pF and three different gains. All these formulas are almost equal for this setting (without R_m, C_m) as is clearly seen from Fig.13.

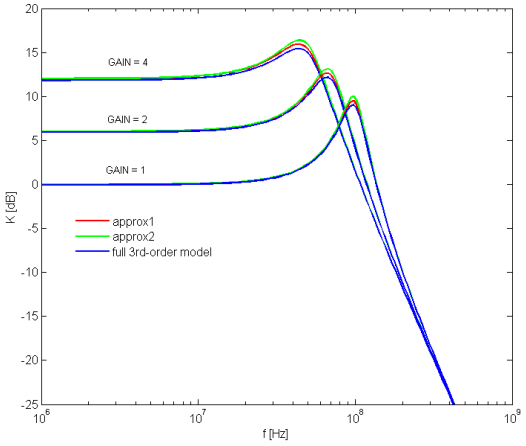


Fig.13. Magnitude responses of the VGA model for different gains.

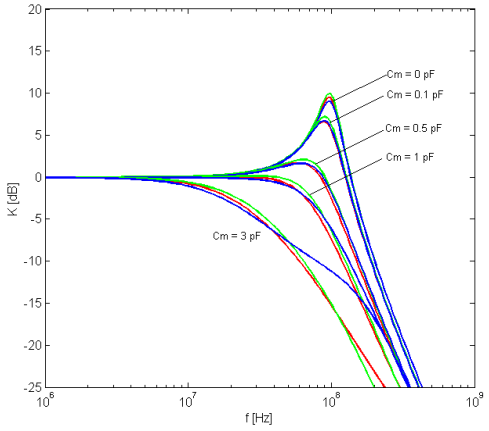


Fig.14. Stepwise change of C_m in compensation network ($R_m = 1$ kΩ).

Above discussed approximate transfer functions (approx1,2) prove that existence of parasitic zero (sufficiently far from ω_{p1}) is not so important as the impact of R_m, C_m on quality factor and distance of complex conjugated poles from imaginary axis as we can see in Fig.14. and equations (7), (15) and (18). Overall gain of the VGA was set to 1. Color of the traces distinguishes both approximations (approx1 - red, approx2 - green) and full 3rd-order model (blue). Value of the capacitor C_m was changed in five steps (0, 0.1, 0.5, 1 and 3 pF) and value of the resistor was set to $R_m = 1$ kΩ. Comparing (18) and (15) to (7), we obtain better (lower) quality (Q_{p1}), this fact causes reduction of the resonant peak.

Fig.15. indicates location of zero and poles of the full 3rd-order model (blue trace in Fig.13. and Fig.14.) for three values of C_m (selected from Fig.14. – for better distinction), i.e. 0.1, 0.5 and 1 pF.

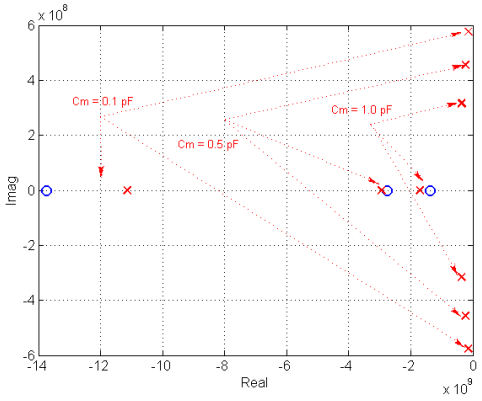


Fig.15. Location of the poles and zeros of the 3rd order mode for C_m changes (0.1, 0.5, 1 pF).

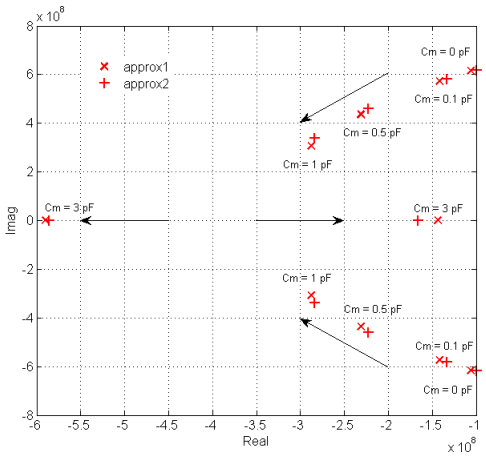


Fig.16. Location of the poles (approx1, approx2) of the small-signal VGA models for C_m changes.

Behavior of the circuit model in the complex space for both approximations (13), (16) is shown in Fig.16. This precaution ensures shattering of complex conjugate poles to two poles on real axis (and reduction of pole quality of course).

The full model of the VGA (Fig.12.) has three poles (two are complex conjugated) and one zero. Location of the zero and poles and magnitude responses for the full 3rd-order model of the closed loop VGA are shown in Fig.17. for two different cases. The first case shows location for optimally selected $C_m = 0.8$ pF (overall $GAIN = 1$). The second case is an example of operation for intentionally critical impact of the second pole shifted to low frequencies ($C_m = 10$ pF). We obtain approximate equations for pole (19) and zero (20) location (included in Fig.18.). The configuration in Fig.18. (for $C_m = 10$ pF) creates 20 dB/dec slope of the magnitude after the first pole (from the left side), then stabilization to the horizontal slope by zero (0 dB/dec) and again fall of the trace (40 dB/dec) after the dominant pole frequency

(complex conjugated). It is typical for pole and zero foregoing the first (dominant) pole given approximately by equations (6), (14) or (17), see Fig.18. The zero and the second pole have quite short distance for small values of C_m. The zero frequency has the form:

$$\omega_{z1} \cong \frac{A}{C_m\left(AR_m - R_o\right)}, \tag{19}$$

which indicates that zero has left-half-plane location for $AR_m > R_o$ and right-half-plane location for $AR_m < R_o$. The boundary between left- and right-half-plane zero is given by $R_m \cong 272\ \Omega$ ($R_o = 16.3$ kΩ, $A = 60$). Approximate second pole frequency which is now (for discussed parameters) below the dominant pole (valid only for high values of C_m – poles shifts in front of the dominant pole; for optimal or no C_m is located above dominant pole) is:

$$\omega_{p2} \cong \frac{g_{mM2}E_g}{C_m\left(1 + g_{mM2}E_gR_m\right)}. \tag{20}$$

Numerical values for our parameters and $C_m = 10$ pF are $f_{p2} = 5.5$ MHz, $f_{z1} = 22$ MHz and $f_{p1} = 129$ MHz. Capacitance $C_m = 0.8$ pF seems to be optimal value for good reduction of the peak and sufficient bandwidth simultaneously, see Fig.19. where gain is changed from 1 to 4 and information about poles, zero and bandwidth is given in the note.

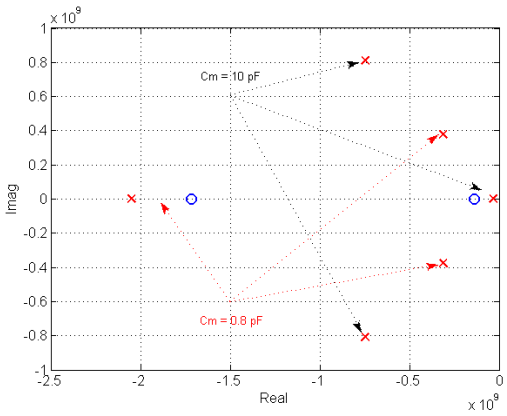


Fig.17. Roots (3rd-order model) of the VGA for $C_m = 0.8$, 10 pF.

Finite gain and frequency features of the inverting amplifier are also very important. Finite gain of the A has impact on dominant pole frequency (influences bandwidth) and real frequency dependent gain of the inverting amplifier A modeled by single pole model $A(s) = A_{pA}\omega_{pA}/(s + \omega_{pA})$, must have pole frequency above (several times higher) all poles of the model in Fig.12.

Proposed VGA with compensation offers some interesting features as was discussed in the introductory section. However, some problems with increasing power consumption and linearity may occur for high input DC offset (hundreds of mV). The DC offset (common mode voltage) causes changes of the bias points which lead to changes of drain currents (and power consumption), linearity (therefore also THD) and the rest of parameters (gain, bandwidth, …). Overall parameters of the VGA depend on this DC offset, first of all for high values of the common mode DC voltage. It is the cost of simplicity and operation without classical differential pair where overall DC current of the differential pair [15] is unchangeable and given by bias tail current source. Therefore, the proposed VGA is suitable for operation with AC coupling (AC amplifier) if almost unchangeable power consumption is required (coupling RC network at the input).

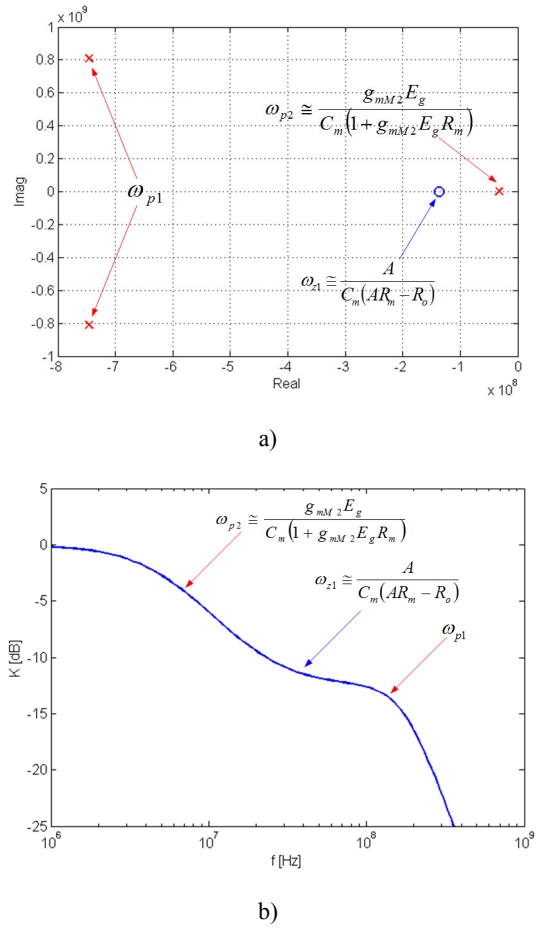


Fig.18. Roots for intentionally critical value of $C_m = 10$ pF ($GAIN = 1$): a) complex plot, b) magnitude.

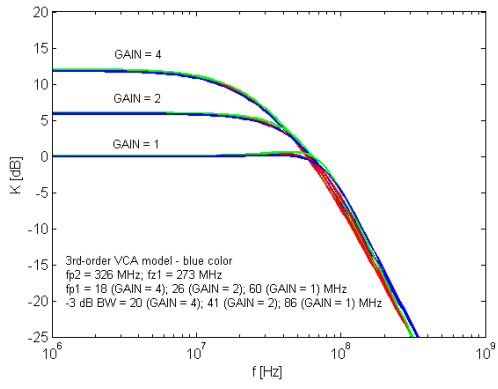


Fig.19. Compensated VGA magnitude responses for different gains ($R_m = 1$ kΩ, $C_m = 0.8$ pF).

Overall output resistance (R_o is part of the feedback loop) is given by:

$$R_{out} \cong \frac{R_o}{g_{mM2} A R_k}\left(1+\frac{R_1}{R_2}\right) = E_g \frac{R_o}{g_{mM2} A R_k}. \quad (21)$$

Actual setting of the gain influences the value of the output resistance (approximately 6–30 Ω in our case for gain between 1 and 5, for example) but the impact can be minimized by a proper value of R_o or A that is given by design of the output section (inverter $-A$).

Influence of the voltage divider R_1, R_2 on overall R_{load} and gain is important for low values of R_2 (i.e., high gains) $R_1' = (R_1 + R_2) \| R_{load}$. In this case, parameter E_g that sets overall gain has the form:

$$E_g(R_2) = \frac{R_l R_2}{R_l(R_o + R_1 + R_2) + R_o(R_1 + R_2)}. \quad (22)$$

6. Electronic Control of VGA

Grounded resistor R_2 can be easily replaced by an electronically controllable equivalent. We used two CMOS transistors in linear/triode (ohmic) regime ($V_{DS} << V_{GS}-V_{th}$) [15].

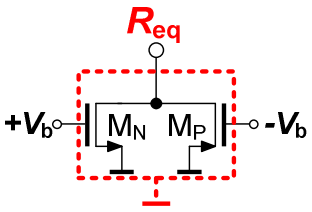


Fig.20. Simple CMOS grounded resistance equivalent.

Both types of transistors (N-MOS and P-MOS) are required for linear operation in both signal polarities (Fig.20.) in order to improve linearity in comparison to one N-MOS. Equivalent resistance can be expressed by the equation [15], [30]:

$$R_{eq} = \frac{1}{g_{oN} + g_{oP}} = \\ = \frac{1}{K_{Pn}\frac{W_n}{L_n}(V_b - V_{th\_n}) + K_{Pp}\frac{W_p}{L_p}(V_b - V_{th\_p})}, \quad (5)$$

considering threshold voltages (V_{th_n} and V_{th_p}) in TSMC LO EPI 0.18 µm models used [31] as +0.37 and -0.39 V, respectively. Technological constants (given by $\mu_0 C_{0X}$) are K_{Pn} = 170.4 µA/V^2 and K_{Pp} = 35.7 µA/V^2. Such implementation (Fig.20.) provides improved linearity in case of a large signal operation [15] when transconductances are equal. This matching is achieved by W adjusting (see different W of both transistors M_7 and M_8).

Electronically controllable CMOS VGA is depicted in Fig.21. Its gain has the form:

$$GAIN = 1 + \frac{R_1}{R_{2eq}} = \\ = 1 + R_1 \cdot \left[K_{Pn}\frac{W_n}{L_n}(V_b - V_{th\_n}) + K_{Pp}\frac{W_p}{L_p}(V_b - V_{th\_p})\right], \quad (6)$$

from which it can be observed that the gain of the VGA is easily adjustable by varying V_b.

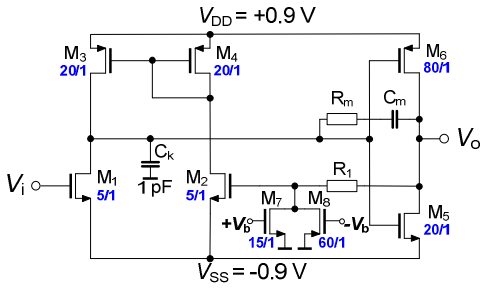


Fig.21. Electronically controllable CMOS VGA.

The CMOS resistor equivalent in Fig.20. is very suitable to control its value in a very wide resistance range (approximately from hundreds of ohms to one hundred of MΩ). High values about hundreds of kΩ and units of MΩ are easily reached by V_b values below threshold voltages of P- and N-MOS transistors. Detail on resistance value dependent on V_b in range from 260 Ω to 10 kΩ can be seen in Fig.22.

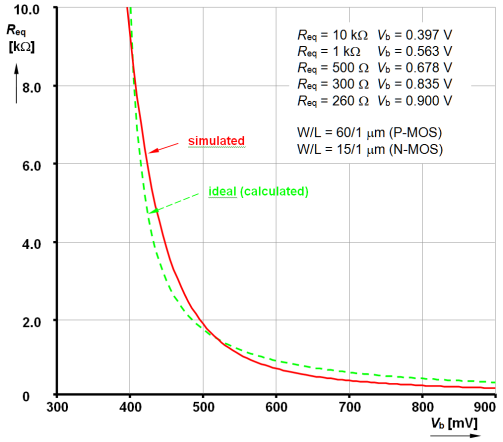
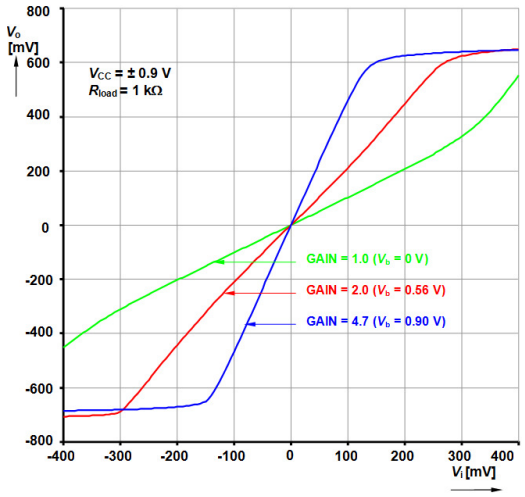
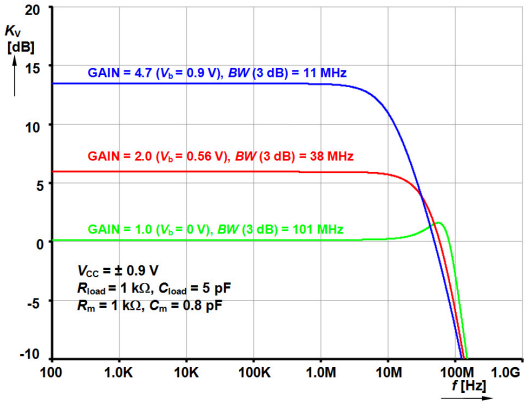


Fig.22. Dependence of CMOS resistor equivalent value in Fig.20. on DC electronically controlled voltage V_b.

The DC and AC performances of the VGA are depicted in Fig.23. Achievable bandwidth (BW) reaches values from 101 to 11 MHz at gain between 1 and 4.7 (R_m = 1 kΩ, C_m = 0.8 pF) for R_{load}=1 kΩ, C_{load} = 5 pF. The minimal achievable resistance value of R_{2eq} is approximately 260 Ω for V_b = 0.9 V (positive supply voltage). Therefore, maximal gain is limited approximately to 4.7. Minimal gain is practically equal to 1, because resistance R_{2eq} is almost infinite for V_b = 0. Dependence of the gain on the control voltage V_b is shown in Fig.24.



a)



b)

Fig.23. Transfer characteristics of VGA for selected different gains set electronically by V_b value: a) DC transfers, b) AC frequency responses.

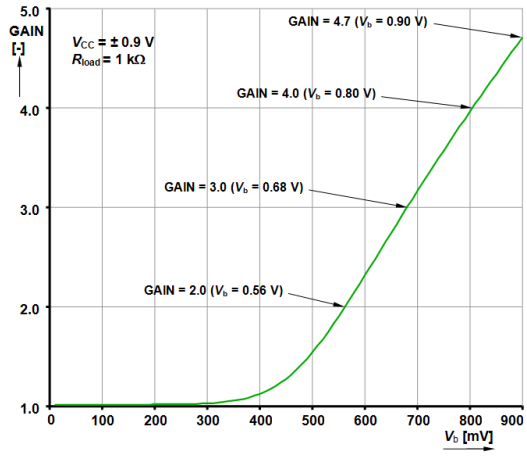


Fig.24. Dependence of gain of VGA on control voltage V_b.

Input resistance of the VGA is almost infinite (gate of N-MOS). The output resistance is dependent on current gain setting. The output resistance value changes between 6 and 30 Ω in the discussed range of V_b (0 – 0.9 V). The overall power consumption of the circuit is not influenced by equivalent resistance control (V_b) and is constant for all the time in simulations. One supply branch has power dissipation about 670 µW (0.9 V, 745 µA) that was estimated by simulations. The W/L aspect ratio of transistors in the output pair (M_5, M_6) has the main impact on power consumption. The sizes of both transistors can be reduced to obtain lower power consumption. However, output resistance significantly increases if smaller transistors M_5, M_6 are used.

7. Comparison of Simulation Results with Hitherto Published Solutions

Parameters obtained from simulations discussed above are summarized in Table 1. The first group consist of controllable high-gain-range amplifiers [18-23] that allow to control the gain in the range about 80 dB (gain can be < 1) or higher. These structures usually contain a high number of transistors, have higher power consumption than other typical examples in Table 1. and utilize differential (transconductance) sections or subsections very often and require biasing (bias current DC sources; in many cases not only one). Our solution has lower number of transistors and lower overall power consumption than circuits discussed in [18-23]. Low range of gain adjusting is the cost for this simplicity, but, as already mentioned, high-gain-range VGA is not the goal of our work.

The second group is focused on voltage followers [24-27] with unity gain. Their power consumption is really very low (µWatts) [24-26] and they are also very simple in many cases [25-27]. Similarly to our solution, circuits in [24-27] do not require differential transconductance sections with tail current sources.

The most similar solution to our proposal (in the view of available features) is the circuit in [26]. The power consumption and number of transistors is low and no biasing (additional source) is required. Unfortunately, gain of this solution from [26] is not controllable.

An example in [28] allows similar type of gain control (gain ≥ 1) as the circuit proposed in this paper. The range of gain adjusting is even higher (35 dB) than in our case. However, power consumption is many times higher, circuit is based on transconductance sections, requires bias sources, and it is also several times more complicated (more than 20 transistors).

Solution in [29] does not allow any gain control. We noted it, because the internal CMOS structure is partially based on an idea similar to our proposal (uses also complementary voltage inverter part).

Based on this comparison, we concluded the following advantages of our solution: proposed circuit uses very low number of transistors, has low power consumption (in comparison to adjustable structures [18-23], [28]), does not require additional bias source(s) as [18-25], [27], [28] and internal conception is not based on typical differential pair approaches [18-20], [22], [23], [28], [29]. We found examples of circuits that combine lower power consumption [24-27], [29] and lower number of transistors [25-27] than our proposal. However, their gain controllability is not possible. Therefore, our approach offers some benefits for specific applications.

Table 1. Comparison of proposed circuit (parameters from simulations) with hitherto published solutions.

Ref.	No. of transistors [-]	Total area [μm^2]	Power supply voltage [V]	Power supply current [mA]	Total power consumption [mW]	Transconductance (differential) sections required	Biasing required (bias current/voltage sources)	Bandwidth [MHz]	Tested DC gain range [dB]
[18]	14	420 000	1.8	11.4	20.5	Yes	Yes	4 - 900	-40 to 55
[19]	16	184 500	1.8	3	5.4	Yes	Yes	up to 350	-42 to 42
[20]	14	N/A	N/A	N/A	10	Yes	Yes	0.01 - 85	0 to 30
[21]	18	150 000	3.3	3.8	12.5	N/A	Yes	20 - 150	-5 to 10
[22]	> 20	400 000	1.8	3.6	6.5	Yes	Yes	40 - 1000	-48 to 36
[23]	> 20	1 000 000	3	12	36	Yes	Yes	50 - 500	-35 to 43
[24]	> 20	N/A	1.8	0.008	0.0144	No	Yes	6	0
[25]	4	8700	± 1.65	N/A	0.066	No	Yes	N/A	0
[26]	5	N/A	1.2	0.0025	0.003	No	No	2.8	0
[27]	3	N/A	2.7	N/A	N/A	No	Yes	2	0
[28]	> 20	680	3.3	N/A	22.3	Yes	Yes	20	0 to 35
[29]	9	14 000	1.2	0.076	0.097	Yes	No	10.2	> 90
Prop.	6 (8)	150 (225)	± 0.9	0.745	1.342	No	No	11-101	0 to 13.5

N/A – not available, not shown or not verified

8. CONCLUSION

We designed simple and unusual CMOS VGA employing only 6 transistors as example of the circuit with typical stability problems due to feedback loop (positive) presented in the structure. Unusual character of the VGA is given by absence of DC bias current source for differential N-MOS pair and implementation of voltage inverter instead of commonly used emitter follower in the second stage. This arrangement of internal sub-blocks is not typical for common opamps (like very similar Miller opamp [15] for example). Despite the positive feedback loop, such simple VGA can really operate sufficiently and steadily (as we confirmed even by experiments) with low controllable range of gain adjusting (the gain increases with decreasing transfer of E_g block, i.e. decreasing value of R_2) or it operates as a simple voltage follower. Frequency features are mainly given by used technological parameters but they can be modified by compensation network (R_m, C_m). We showed that compensation of possible instability issues can be solved by really simple additional passive RC circuitry also in such potentially not-beneficial solution at the first sight, which was one of the important goals of this work. Proposed solution is suitable mainly for AC signal processing and due to single-ended (non-differential) input has also some disadvantages. However, its utilization depends on actual designer's requirement and also such circuit may offer interesting and useful features, as we discussed in the text. Designer is also responsible for selection of final gain control (electronically adjustable equivalent of grounded resistor R_2 -MOS in triode regime [30], for example if linearity limitation of used MOS equivalent is sufficient for resulting application). Simple change of gain in the feedback loop (value of grounded resistor) allows control of gain from 1.1 to 7 by varying resistor R_2 from 10 kΩ to 100 Ω (as was confirmed by measurement). Additional measurement results with commercially available CMOS elements also confirmed the expected behavior. Proposed circuit is suitable to serve as a sub-block of more complex active elements (see for example [1], [12]) and to provide adjustability in application circuits (filters, oscillators, inductance simulators, etc.). Parameters of the VGA in the simulated and the measured (different technology) case are summarized in Table 2.

Table 2. Summarization of parameters obtained from simulations and measurements of the VGA.

	simulated (TSMC 0.18 μm)	measured (ALD1106/7)
No. of transistors [-]	6 (8)	6
Total area [μm^2]	150 (225)	-
Power supply voltage [V]	± 0.9	± 1.5
Total power consumption [mW]	1.5	1.5-1.8
Input resistance [MΩ] @ 1 MHz	3.7	-
Input capacitance [fF]	43	-
Output resistance [Ω] @ gain → 1 (2)	6 (12)	-
Transit frequency (GBW) [MHz] @ gain → 1 (2) (R_{load} = 1 kΩ, C_{load} = 5 pF, R_m = 1 kΩ, C_m = 0.8 pF)	90 (37)	5.04 (2.30)
Tested gain range [-]	1.1 - 10	1.15 - 7.04
THD [%] @ gain → min., max.; V_{inp} = 100 mV$_{P-P}$ (1 kHz)	0.13, 0.63	0.06, 1.21

Application of the proposed VGA in the low-power and low-gain-range continuously controllable voltage amplifiers useful for design of oscillators (with requirements of oscillation condition fulfillment – voltage gain in the loop around 2 [12], [34]), working in base-band and intermediate frequency bands (up to several MHz), is expected. Studied

VGA can be used as really simple voltage buffer very easily (full feedback, $R_2 \to \infty$), which is also a required subpart of many systems (design of oscillators and filters) and modern active devices [12], [34]. Therefore, independency of the power consumption on gain setting is a really important feature for low-power solutions, even if some limitations are evident from the used concepts. Minimization of the power consumption is the most important feature for many battery supplied systems today, where solutions of amplifiers, etc. without requirement of biasing sources, can be really interesting. Presented solution in function of voltage buffer and VGA was designed as a simpler replacement of CMOS structure of voltage buffer and electronically adjustable amplifier in [34] (see Fig.2. – concept; and Fig.14. – CMOS implementation in [34]) in frame of advanced active devices (their subparts).

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