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A Cost-effective Method for Resolution Increase of the Two-stage Piecewise Linear ADC Used for Sensor Linearization

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A cost-effective method for resolution increase of a two-stage piecewise linear analog-to-digital converter used for sensor linearization is proposed in this paper. In both conversion stages flash analog-to-digital converters are employed. Resolution increase by one bit per conversion stage is performed by introducing one additional comparator in front of each of two flash analog-to-digital converters, while the converters' resolutions remain the same. As a result, the number of employed comparators, as well as the circuit complexity and the power consumption originating from employed comparators are for almost 50 % lower in comparison to the same parameters referring to the linearization circuit of the conventional design and of the same resolution. Since the number of employed comparators is significantly reduced according to the proposed method, special modifications of the linearization circuit are needed in order to properly adjust reference voltages of employed comparators.

Keywords: Analog-digital conversion, comparator count, resolution increase, sensor linearization.

1. INTRODUCTION

One of the most common causes of a measuring system low accuracy is nonlinearity of a sensing element. There are many techniques developed to compensate a sensor nonlinearity, but the linearization with a two-stage piecewise linear analog-to-digital converter (two-stage PWL ADC) has proved to be one of the most effective [1]-[4]. In particular, the sensor linearization is performed simultaneously with the signal digitalization, i.e. at digital conversion speed. In this manner, the processing time, the power consumption and the production costs of a smart sensor system containing the two-stage PWL ADC are reduced [2]. However, linearization of a sensor, i.e. linearization of its transfer function can be performed by using some other techniques, analog or digital, depending on whether the linearization of a sensor is performed before or after analog-to-digital conversion, respectively. An example of an analog linearization technique is application of a neural network, as it is shown in [5]. In paper [5], application of a special time delay neural network for linearization of an elastomagnetic sensor used for measurement of a massive pressure force is suggested. The major drawbacks of elastomagnetic sensors are nonlinear transfer function and hysteresis, which causes ambiguity of the transfer function, i.e. prevents the exact conversion of sensor output electric voltage into one measured force value. In paper [5], the implementation of the neural network, as the measurement data conditioning block, solves the problem with mentioned conversion and reduces sensor errors. In particular, the elastomagnetic sensor nonlinearity is reduced from the value of approximately 6 % to the value of approximately 2 % by using the proposed time delay neural network. However, this result is not obtained without any difficulties since the time delay neural networks require many training examples before a satisfactory level of accuracy is obtained. This additional time period, used for the preparation of the time delay neural network for sensor linearization, is not required in the case when sensor linearization is performed by using the two-stage PWL ADC.

When a digital signal processing method is considered for the sensor linearization, limitations such as small memory or small computing capacity become important. These limitations are especially significant when the mathematical expression of a sensor transfer function is unknown, i.e. when it needs to be approximated. However, these limitations are avoided when the two-stage PWL ADC is used. As an approximation method Newton interpolation polynomials can be employed to approximate the unknown function between known pairs of sensor input/output values (respected nodes). An example of a digital sensor linearization method is the application of a microcomputer, in which the inverse function of the approximated sensor transfer function is embedded [6].

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In papers [2]-[4], different circuit designs of the two-stage PWL ADC are proposed for a sensor linearization and digitalization of a sensor output signal. Common for all proposed designs is that in both conversion stages flash ADCs are employed. The reference resistor ladder, comparators and the priority encoder are the main parts of the flash ADC architecture [7]. Also, the transfer function of the first stage flash ADC is a piecewise linear approximation of a nonlinear function inverse to a sensor transfer function. In this manner, the transfer function of the circuit section starting from a sensor input and ending with the first stage flash ADC output is linear. In other words, sensor nonlinearity is compensated in the first stage of analog-to-digital conversion. The piecewise linear transfer function of the first stage flash ADC is composed of linear segments of unequal width bounded by the points that are called break voltages [2]-[4]. Break voltages are the reference voltages of the comparators that are composing the first stage piecewise linear flash ADC.

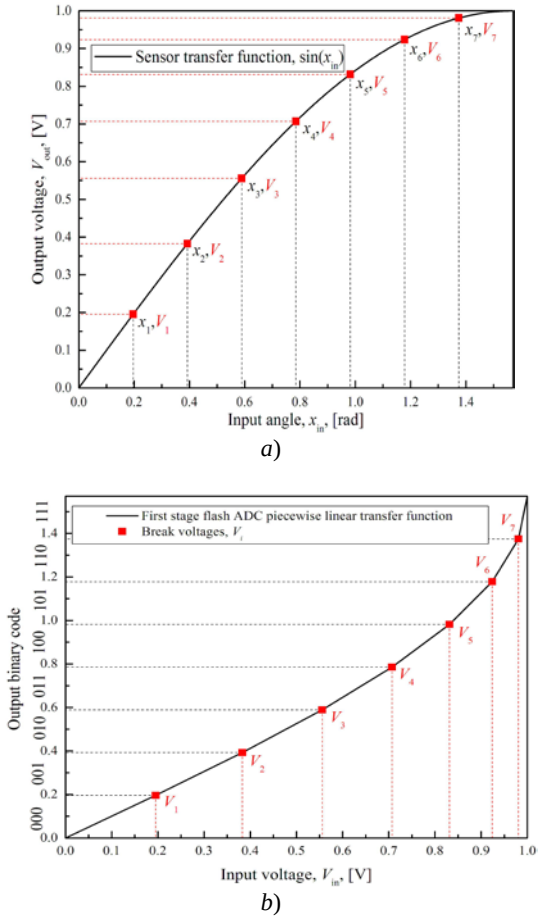

Fig.1. a) An optical rotary encoder transfer function, sin(x). b) The piecewise linear approximation of arcsin(x) function as the transfer function of the 3-bit first stage piecewise linear flash ADC, with the break voltages V_i.

The most important advantage of the two-stage PWL ADC is that it can be easily adapted for linearization of any sensor type. This adaptation is performed by changing the transfer function of the first stage piecewise linear flash ADC. In particular, break voltages need to be changed in order to fit the first stage flash ADC transfer function to correspond to the piecewise linear approximation of a function inverse to a sensor transfer function. Thus, in paper [2], humidity sensor nonlinearity is treated and in a high percentage eliminated by adjusting break voltages so the first stage flash ADC transfer function corresponds to the piecewise linear approximation of a function inverse to the humidity sensor transfer function. The same principle is applied to the linearization of a magneto-resistive sensor bridge [3] and an optical rotary encoder [4] used for angular position determination of rotating objects.

The implementation of the second conversion stage comes from the need to reduce the quantization error introduced in the first conversion stage, which simultaneously increases the measurement resolution and the accuracy of the measurement results.

For better understanding of the linearization process, in Fig.1.a) is given an optical rotary encoder transfer function modelled with a mathematical function sin(x) [4], and in Fig.1.b) is given a corresponding piecewise linear approximation of its inverse function arcsin(x). In accordance with the previous statements, the piecewise linear approximation of the function arcsin(x) is the first stage flash ADC transfer function. From Fig.1.b), it can be observed that the input range of the 3-bit first stage piecewise linear flash ADC is divided into eight linear segments of unequal width. These segments are bounded by the break voltages V_i, i=1, 2,…, 7. These voltages are obtained at the optical encoder output for the input angle values x_i [rad], i=1, 2, …, 7, that are uniformly distributed between boundaries of the optical encoder input range that is spanning from 0 to π/2 [rad] (see Fig.1.a)). The sine values of selected angles represent the break voltages that are non-uniformly distributed between 0 and 1V, which is the maximal voltage that can be obtained at the optical encoder output. At the same time, the optical encoder output range represents the 3-bit first stage piecewise linear flash ADC input range and the break voltages V_i are the comparators' reference voltages. The output of the first stage flash ADC is a 3-bit digital code word. To conclude, the piecewise linear flash ADC transfer function is chosen with a goal to provide linear relation between the output digital code and the measured angle.

In papers [2]-[4], the reference resistor ladder that is setting up the reference voltages of the comparators of the first stage piecewise linear flash ADC, consists of resistors with mutually unequal resistances since the piecewise linear flash ADC input range consists of linear segments of unequal width. In addition, in papers [2] and [3], resistors are variable in order to provide the change of break voltages when the type of a sensor is changed. In any case, the linearization starts by comparing a sample of an analog input voltage (sensor output voltage) with break (reference) voltages. In this manner, the most significant bits of the final digital output code are obtained. These bits represent the linear segment of the first stage piecewise linear flash ADC input range to which the sample belongs. Break voltages, which are bounding the resolved segment, are the boundaries of the input range of the second stage flash ADC. The second stage flash ADC has linear transfer

function, i.e. its input range is composed of uniform cells of equal width. For this reason, its reference resistor ladder consists of non-variable resistors with mutually equal resistances. By using the second stage flash ADC the remaining bits of the final digital output code are obtained, i.e. the measurement resolution is increased and the measurement accuracy is improved.

In this paper, a cost-effective method for resolution increase of the previously described two-stage PWL ADC is proposed. The proposed method provides resolution increase by one bit per conversion stage by introducing one additional comparator in front of each employed flash ADC, while ADC converters' resolutions remain the same. The cost-effectiveness of the proposed method is reflected in the fact that the complexity and the power consumption, originating from the employed comparators, are lower in comparison to the two-stage PWL ADC where the resolution increase is performed by increasing flash ADCs' resolutions, i.e. when the conventional method for the resolution increase is applied.

More details about the proposed method for the two-stage PWL ADC resolution increase and its comparison to the conventional method are given in the following section of the paper. The numerical results concerning the number of employed comparators, as the most power consuming components of the circuit, are obtained. After the analysis of the obtained numerical results, the conclusions are derived.

2. THE PROPOSED METHOD

Flash type ADCs provide the highest conversion speed among other ADC types, but at the cost of higher complexity and higher power consumption [7]. The number of comparators that are composing the flash ADC is 2^N-1, where N stands for the flash ADC resolution, so the flash type ADC has a significant drawback that the resolution increase by one bit doubles the number of comparators that are composing its circuit [7]. Due to its emerging and significant application in sensor linearization, any design modification that can eliminate or minimize known drawbacks caused by the resolution increase would be of great importance. In order to perform a resolution increase in a cost-effective manner, in [8] and [9] the authors suggest introduction of one or more comparators before flash ADC to split its input range into two, four, eight or more equal sections. In this manner, only one additional comparator is needed to increase the resolution by one bit, while the flash ADC resolution remains the same. In this paper, the resolution increase by one bit per conversion stage is performed by introducing one comparator in front of each of two flash ADCs that are composing the two-stage PWL ADC. In contrast to [8] and [9], in this paper, a comparator introduced in the first conversion stage does not split the flash ADC input range into two equal sections. In other words, difference between our design of the first stage flash ADC and the flash ADC designs proposed in [8] and [9] is in the value of a reference voltage of the comparator introduced in the first conversion stage. Consequently, due to the specific manner in which this voltage is set, additional modifications of the reference resistor ladder of the first stage flash ADC are required. In the second stage of conversion the additional comparator splits the flash converter input range (bounded by the break voltages determined in the first conversion stage) into two equal sections. To adjust the reference voltage of this comparator to be in the middle between boundaries of the selected segment, the conventional design of the second conversion stage is altered as well.

As already stated, the flash ADC has the advantage of being very fast because the conversion occurs in a single cycle, and the disadvantage that it requires a large number of comparators that need to be carefully matched and properly biased. However, the conversion time does not increase with the increase of resolution. When higher resolution and smaller power consumption for a given resolution are required, multistage conversion is employed. In this paper two-stage conversion is exploited. The two-stage principle reduces the number of bits to be converted into two smaller groups. The proposed method for the modification of the two-stage PWL ADC combines principles from SAR and flash architectures inside one conversion stage. While a flash converter uses many comparators to convert in a single cycle, a SAR converter uses a single comparator over many cycles to make its conversion [7]. The proposed modifications of the two-stage architecture imply the inclusion of one comparator per conversion stage to provide conversion and linearization of a sensor using lower-resolution flash ADCs. In the proposed design, one complete conversion process is finished after two conversion cycles per conversion stage (one comparator plus one flash ADC), i.e. there are four conversion cycles in one complete conversion process. This approach reduces the number of comparators and reduces the logic complexity compared to a conventional two-stage PWL ADC. The trade-off results in a slower conversion speed compared to conventional two-stage PWL ADC. However, measurement results are still obtained faster when the linearization and the analog-to-digital conversion are performed simultaneously, than by using an analog/digital linearization method that is performed before/after the analog-to-digital conversion.

In order to get a better insight into differences between the conventional and the proposed design of the two-stage PWL ADC, we have assumed the same initial circuit resolution of 10 bits with the 2-bit first stage and the 8-bit second stage.

Fig.2. illustrates the 12-bit two-stage PWL ADC of the conventional design composed of a 3-bit piecewise linear flash ADC and a 9-bit differential flash ADC, while Fig.3. and Fig.4. present the proposed designs of the first (1+2)-bit conversion stage and the second (1+8)-bit conversion stage, respectively. Also, these figures are showing circuits when the variation of break voltages, due to replacement of a sensor, is not expected.

Higher complexity and power consumption of the circuit shown in Fig.2. originate from larger number of comparators employed in comparison to the proposed design of the two-stage PWL ADC of the same resolution. This is the main reason to avoid the conventional approach for the two-stage PWL ADC resolution increase. In comparison to the conventional design of the 3-bit first conversion stage, where seven comparators are employed, in the proposed design of the 3-bit first conversion stage four comparators

are employed, including the newly introduced comparator C1 (Fig.3.). However, in both cases, seven reference (break) voltages are needed and are mutually equal for both designs, but the reference resistor ladders that are setting them up are different. For example, the reference voltage V_{ref1} of the additional comparator C1 is equal to the central break voltage V_4 of the 3-bit piecewise linear flash ADC of the conventional design.

In addition, the complexity and production costs of the conventional circuit are higher in comparison to the proposed circuit since the 3-bit first stage (Fig.2.) employs the 3-bit priority encoder and two analog multiplexers 8-to-1. These blocks require a higher number of logic circuits than it is needed for the realization of the 2-bit priority encoder, two analog multiplexers 2-to-1 and two analog multiplexers 4-to-1 used in the (1+2)-bit first conversion stage of the proposed circuit (Fig.3.).

In the first conversion stage of the proposed circuit (Fig.3.), the comparator C1 and the 2-bit flash ADC1 (N_1=2) provide the 3-bit resolution, while in the second stage (see Fig.4.) the comparator C2 and the 8-bit differential flash ADC2 (N_2=8) provide the 9-bit resolution. Depending on the output bit of the comparator C1, the reference voltages of the 2-bit flash ADC1, which employs three comparators, are V_3, V_2 and V_1, or V_7, V_6 and V_5. As it can be noted, seven reference voltages are needed (V_{ref1}=V_4 and V_1, V_2, V_3, V_5, V_6 and V_7), but the reference resistor ladder that is setting them up is different from the conventional design shown in Fig.2.

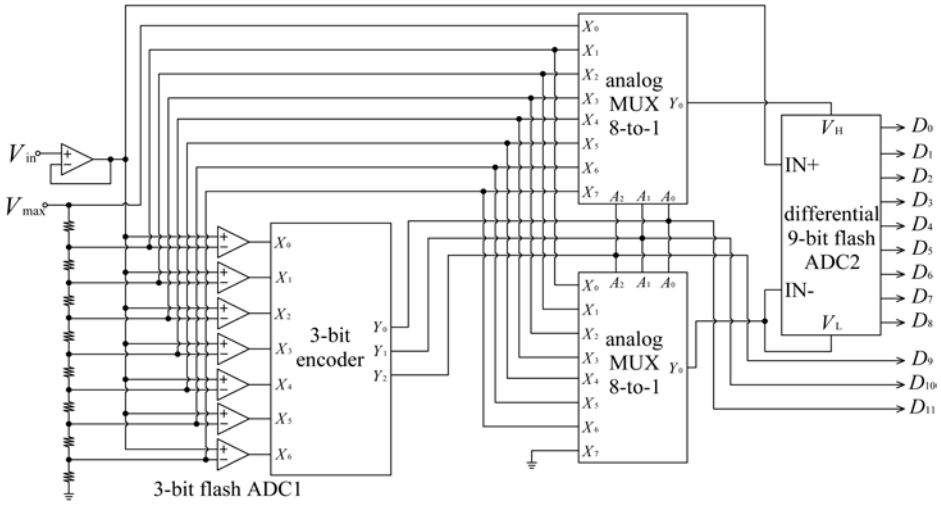

Fig.2. The 12-bit two-stage PWL ADC with the conventional design (both conversion stages).

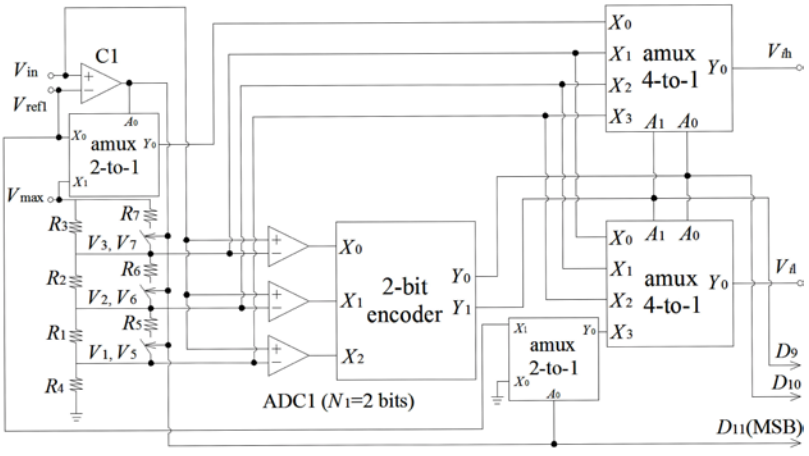

Fig.3. The proposed design of the first (1+2)-bit analog-to-digital conversion stage of the 12-bit two-stage PWL ADC.

The reference voltages of comparators employed in the first conversion stage correspond to measured parameter values that are obtained by dividing the sensor input range into $2^{(N1+1)}$ uniform segments (as an example see Fig.1.a)). However, most outer boundaries of the sensor input range are not used for the calculation of the reference voltages. For example, for the 3-bit first conversion stage (N_1=2) we have 2^3=8 segments and nine segment boundaries. When the first and the last boundary (the boundaries of the sensor input range) are excluded, seven measured parameter values and seven voltages at the sensor output are obtained. The obtained (break, reference) voltages are not equidistant due to the sensor nonlinearity. Reference voltage V_{ref1} of the comparator C1 (Fig.3.) corresponds to the voltage obtained at the output of the sensor when the value of a measured parameter x is equal to one half of the sensor input range.

This voltage is given with the following expression:

$$V_{\text{ref1}} = f_s\left[\frac{\left(x_{\min} + x_{\max}\right)}{2}\right], \tag{1}$$

wherein f_s is a monotonically rising nonlinear transfer function of the sensor, $x_{\min}$ is the lower bound and $x_{\max}$ is the upper bound of the sensor input range. To simplify the explanation of the proposed method for the resolution increase of the two-stage PWL ADC without disturbing its basic principles it is assumed that the lower bound $x_{\min}$ is equal to 0.

The reference voltages of comparators that are composing the 2-bit flash ADC1 are derived from the maximal sensor output voltage $V_{\max}$. For this purpose special design of the reference resistor ladder is proposed (Fig.3.). The voltage $V_{\max}$ is obtained at the output of the sensor when the measured parameter x reaches the maximal value (upper bound of the sensor input range):

$$V_{\max} = f_s\left[x_{\max}\right]. \tag{2}$$

The input range of the 3-bit first conversion stage goes from 0 to $V_{\max}$, while the input range of the 2-bit flash ADC1 varies according to the comparator C1 output bit, i.e. it goes from 0 to V_{ref1} or from V_{ref1} to $V_{\max}$. To adjust boundaries of the 2-bit flash ADC1 input range, two analog multiplexers 2-to-1, controlled by the C1 output bit, are introduced (see Fig.3.). In addition, the switches controlled by the output bit of the comparator C1 are introduced to provide the generation of corresponding reference voltages. Also, the modified resistor ladder contains one resistor less in comparison to the resistor ladder of the 3-bit first stage flash ADC of the conventional design (see Fig.2.).

When the sample of the sensor output voltage V_{in} belongs to lower section ($V_{\text{in}} \le V_{\text{ref1}}$), the output bit of C1 is 0 and the switches in the resistor ladder are open. In this case, the input range of the 2-bit flash ADC1 goes from 0 to the reference voltage V_{ref1}. For the resolved section, on comparators' inputs are brought reference voltages V_3, V_2 and V_1 obtained using the resistor ladder composed of resistors R_3, R_2, R_1 and R_4. When the sample V_{in} belongs to higher section ($V_{\text{in}} > V_{\text{ref1}}$), the output bit of the comparator C1 is 1. The obtained logic value closes the switches and changes the values of reference voltages. In this case, the reference voltages V_7, V_6 and V_5 are obtained by forming parallel connections between the resistors R_3 and R_7, R_2 and R_6 and R_1 and R_5, respectively. Since the resistances R_7, R_6 and R_5 are chosen to be less than the resistances R_3, R_2 and R_1, respectively, the equivalent resistances of their parallel connections are less than R_3, R_2 and R_1, respectively. As a result, higher reference voltages are obtained and brought on comparators' inputs ($V_5 > V_1$, $V_6 > V_2$ and $V_7 > V_3$). The output bit of C1 is the MSB bit ($D11$ bit from Fig.3.). When MSB bit is 0, the resistances of the currently employed resistors (in this case R_3, R_2, R_1, and R_4 that has fixed and known in advance value) can be calculated as follows:

$$R_i = \frac{V_{i+1} - V_i}{V_1} \cdot R_{2^{N_1}}, \text{ for } i = 1, \ldots, 2^{N_1} - 2, \tag{3}$$

and

$$R_i = \frac{V_{\max} - V_i}{V_1} \cdot R_{2^{N_1}}, \text{ for } i = 2^{N_1} - 1, \tag{4}$$

wherein

$$V_i = f_s\left(x_i\right) \text{ and } x_i = \frac{x_{\max}}{2^{N_1+1}} \cdot i. \tag{5}$$

However, when MSB bit is 1, the resistances of the newly employed resistors (in this case R_7, R_6 and R_5) can be calculated as follows:

$$R_i = \frac{R_{i-2^{N_1}}\left(V_{i+1} - V_i\right)}{R_{i-2^{N_1}} \cdot V_{1+2^{N_1}} - R_{2^{N_1}}\left(V_{i+1} - V_i\right)} \cdot R_{2^{N_1}}, \quad \text{for } i = 1 + 2^{N_1}, \ldots, 2^{N_1+1} - 2, \tag{6}$$

and

$$R_i = \frac{R_{i-2^{N_1}}\left(V_{\max} - V_i\right)}{R_{i-2^{N_1}} \cdot V_{1+2^{N_1}} - R_{2^{N_1}}\left(V_{\max} - V_i\right)} \cdot R_{2^{N_1}}, \quad \text{for } i = 2^{N_1+1} - 1, \tag{7}$$

wherein again

$$V_i = f_s\left(x_i\right) \text{ and } x_i = \frac{x_{\max}}{2^{N_1+1}} \cdot i. \tag{8}$$

The resistor R_i, for $i=2^{N1}$, i.e. R_4 for the particular case, has fixed value that is independent of the sensor transfer function, i.e. this resistor is not tunable (non-variable).

As already mentioned, two analog multiplexers 2-to-1 are introduced to provide the change of the 2-bit flash ADC1 input range boundaries. In addition, these multiplexers, controlled by the output of the comparator C1, are setting up the highest possible value for the higher segment boundary (V_{ref1} or $V_{\max}$), and the lowest possible value for the lower segment boundary (0 or V_{ref1}). These values are brought on corresponding inputs of two analog multiplexers 4-to-1 ($X0$ and $X3$) together with the corresponding reference voltages. A segment, to which the input sample V_{in} belongs, is determined by the 2-bit flash ADC1, while two analog multiplexers 4-to-1 resolve boundaries of the determined segment according to the 2-bit flash ADC1 output bits ($D10$ and $D9$). The lower bound is marked with $V_{i\text{l}}$ (i=1, 2,…, 2^{N1}) and the higher bound is marked with $V_{i\text{h}}$ (i=1, 2,…, 2^{N1}). By the end of the first conversion stage, boundaries of a segment to which the input sample V_{in} belongs and three most significant bits of the final output digital code are obtained.

To increase the resolution of the second conversion stage by one bit, the additional comparator C2 is introduced (Fig.4.). Since the flash ADC2 has linear transfer function, the reference voltage V_{ref2} is chosen to be in the middle

between voltages V_{il} and V_{ih}, i.e. similar to the solutions proposed in [8] and [9]. The voltage V_{ref2} is obtained from voltages V_{il} and V_{ih} that are brought on the inputs of the passive averaging circuit composed of two resistors of equal resistances R, and can be expressed as follows:

$$V_{\text{ref2}} = \frac{\left(V_{il} + V_{ih}\right)}{2}. \tag{9}$$

Two multiplexers 2-to-1 (Fig.4.), controlled by the output bit of the comparator C2 ($D8$ bit of the final digital output code), select the boundaries of the corresponding section to which the input sample V_{in} belongs. Similar to the first conversion stage, for $V_{\text{in}} \leq V_{\text{ref2}}$, the output bit of C2 is 0 and the boundaries of the input range of the 8-bit differential ADC2 are V_{il} (lower bound) and V_{ref2} (higher bound). For $V_{\text{in}} > V_{\text{ref2}}$, the output bit of C2 is 1 and the boundaries of the input range of the 8-bit differential ADC2 are V_{ref2} (lower bound) and V_{ih} (higher bound). After the selected boundaries are brought to the differential inputs of the 8-bit flash ADC2 (V_{l} and V_{h}), the remaining bits (from $D7$ to $D0$) of the final output digital code are resolved.

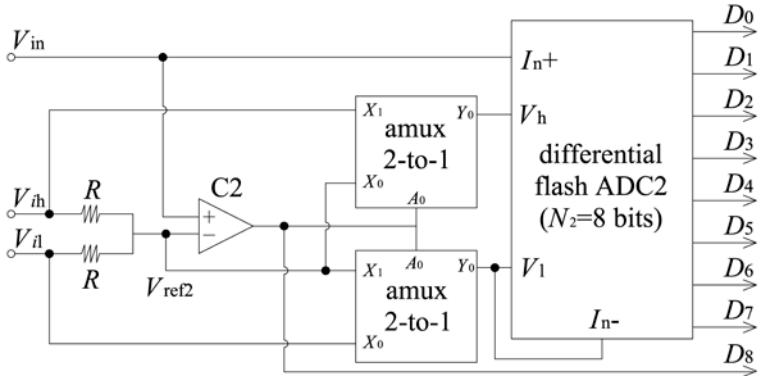

Fig.4. The proposed design of the second (1+8)-bit analog-to-digital conversion stage of the 12-bit two-stage PWL ADC.

3. THE NUMERICAL RESULTS

The previously described method provides the resolution increase of the two-stage PWL ADC from 10 to 12 bits by using the 2-bit flash ADC1, the 8-bit flash ADC2 and two additional comparators, C1 and C2. The conventional approach of performing the resolution increase implies the employment of the 3-bit flash ADC in the first stage, and the 9-bit flash ADC in the second stage, i.e. two flash ADCs of increased resolutions. In the latter case, the total number of comparators employed is much greater [7]. To prove the cost-effectiveness of the proposed method, we have calculated the total number of employed comparators and compared it with the corresponding value obtained for the conventional approach. Considering that the number of comparators composing one N-bit flash ADC is 2^N-1 [7], the total number of comparators composing the two-stage PWL ADC after the resolution is increased by one bit per conversion stage by using the proposed method n_{cp} is:

$$n_{cp} = 1 + \left(2^{N_1} - 1\right) + 1 + \left(2^{N_2} - 1\right), \tag{10}$$

wherein N_1 and N_2 are the first and the second stage resolutions, respectively, before the resolution increase. However, the total number of comparators composing the two-stage PWL ADC after the resolution is increased by one bit per conversion stage by using the conventional method n_{cc} is:

$$n_{cc} = 2^{(N_1+1)} - 1 + 2^{(N_2+1)} - 1, \tag{11}$$

wherein N_1 and N_2 are the first and the second stage resolutions, respectively, before the resolution increase. A significant portion of complexity and power consumption of the two-stage PWL ADC originates from employed comparators. A difference in the number of employed comparators reveals a difference in the complexity and power consumption between two discussed designs of the two-stage PWL ADC. The following expression shows the relative difference in percentage between numbers of comparators employed by these two designs of the two-stage PWL ADC:

$$\delta_r\left[\%\right] = \left(\frac{n_{cc} - n_{cp}}{n_{cc}}\right) \cdot 100 = \frac{1}{2}\left(1 - \frac{1}{2^{N_1} + 2^{N_2} - 1}\right) \cdot 100 \cdot \tag{12}$$

The previous expression is derived by substituting n_{cp} and n_{cc} with the expressions (10) and (11), respectively. The numeric values of the previously defined parameters are given in Table 1 for different combinations of resolutions N_1 and N_2 of the flash ADC1 and ADC2, respectively.

Table 1. The two-stage PWL ADC parameters in relation to the resolutions N_1, N_2 and applied method for the resolution increase.

1+N_1 [bit]	**1+N_2 [bit]**	**n_{cp}**	**n_{cc}**	**n_{cc}-n_{cp}**	**δ_r [%] (12)**
1+2	1+8	260	518	258	49.807
1+2	1+10	1028	2054	1026	49.951
1+2	1+12	4100	8198	4098	49.988
1+2	1+14	16388	32774	16386	49.997
1+4	1+8	272	542	270	49.816
1+4	1+10	1040	2078	1038	49.952
1+4	1+12	4112	8222	4110	49.988

By analyzing the results given in Table 1., one can conclude that the proposed design employs a significantly lower number of comparators. The column n_{cc}-n_{cp} shows a difference in the number of employed comparators, while the last column shows how much, in percentage, is the number of comparators n_{cp} lower than the number of comparators n_{cc}. These values give an estimation of a difference in the power consumption caused by the comparators employed in these two circuit designs. In all cases presented in Table 1., the relative difference is almost 50 %. All the previous statements go in favor of the proposed method stating that it is almost two times more cost-effective in comparison to the conventional method for the resolution increase of the two-stage PWL ADC, when initial resolutions N_1 and N_2 of the first and the second conversion stage, respectively, are in both cases the same. In other words, the complexity, production costs and the power consumption of the proposed circuit are lower in comparison to the circuit where the resolution increase is performed in the conventional manner.

Another observation is that the relative difference δ_r increases with the increase of the overall resolution ($1+N_1+1+N_2$). In addition, δ_r becomes closer to 50 % when N_2 increases and N_1 decreases in a manner that the overall resolution remains the same. This is an advantage since the first conversion stage has higher complexity in comparison to the second stage, i.e. by reducing N_1 the first stage complexity is reduced as well. On the other hand, by utilizing lower resolution in the first conversion stage the effect of linearization becomes mitigated. Due to previous reasons, the compromise between the complexity and the linearization effect of the first conversion stage needs to be made.

4. Conclusion

A special method for resolution increase of the two-stage PWL ADC used for sensor linearization has been presented. The proposed method is cost-effective in terms of power consumption and complexity of the two-stage PWL ADC circuit since its application requires a lower number of comparators in comparison to the conventional method for the resolution increase performed by increasing resolutions of flash ADCs. These benefits are achieved by introducing just one additional comparator per conversion stage to increase the conversion stage resolution by one bit. To increase the resolution and perform the sensor linearization properly, the reference voltages of the comparators are set using the customized resistor networks developed for this particular purpose. It is important to note that, for the same resolution, the total number of employed comparators is almost two times smaller in comparison to the conventional method for the resolution increase. This result justifies the introduction of the proposed modifications in the conventional design of the two-stage PWL ADC circuit.

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