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Mixed-mode Method Used for Pt100 Static Transfer Function Linearization

Jelena Jovanović, Dragan Denić

Department of Measurements, Faculty of Electronic Engineering, University of Niš, Aleksandra Medvedeva, 14, 18000, Niš, Serbia, jelena.jovanovic@elfak.ni.ac.rs

Pt100 is a resistance temperature detector characterized by a relatively linear resistance/temperature relationship in a narrow temperature range. However, the Pt100 sensor shows a certain degree of static transfer function nonlinearity of 4.42 % in the range between -200 °C and 850 °C, which is unacceptable for some applications. As a solution to this problem, a mixed-mode linearization method based on a special dual-stage piecewise linear ADC design is proposed in this paper. The first stage of the proposed dual-stage piecewise linear ADC is performed with a low-complex and low-power flash ADC of a novel sequential design. The novelty of the proposed sequential design is reflected in the fact that the number of employed comparators is equal to the flash ADC resolution. The second stage is performed with a delta-sigma ADC with a differential input and differential reference. Using the 6-bit flash ADC of novel design and the 24-bit delta-sigma ADC, the nonlinearity error is reduced to $2.6 \cdot 10^{-3}$ %, in the range between -200 °C and 850 °C. Two more ranges are examined, and the following results are obtained: in the range between 0 °C and 500 °C, the nonlinearity error is reduced from 1.99 % to $5 \cdot 10^{-4}$ %, while in the range between -50 °C and 150 °C, the nonlinearity error is reduced from 0.755 % to $2.15 \cdot 10^{-4}$ %.

Keywords: Flash ADC, mixed-mode method, nonlinearity compensation, Pt100 static transfer function, sequential design.

1. INTRODUCTION

Temperature is the most frequently measured and controlled physical quantity. The importance of temperature measurement can be seen in health care applications, industry, food processing, environmental monitoring, space explorations, etc. A temperature value can be measured using a variety of temperature sensors: thermistors, thermocouples, resistance temperature detectors (RTDs), infrared sensors, etc., where each sensor type is suitable for the specific application [1], [2], [3]. Among these sensors, platinum RTDs (PRTDs) are the most commonly used due to their high accuracy, best long-term stability, wide temperature range (between -200 °C and 850 °C), negligible resistance drift during the time, and easiness of production at a reasonable cost [4]. However, their disadvantages include lower sensitivity, longer response time, and susceptibility to self-heating. Although PRTDs exhibit better linearity than thermistors and thermocouples, a static transfer function of, for example, Pt100 sensor still has a certain level of nonlinearity. There are applications, such as reference sensors for calibration or research and development applications in science and industry, where sensor linearity and measurement accuracy in a wide temperature range are demanded. For this reason, sensor linearization would be of great importance for measurement error reduction.

Different methods for the nonlinearity compensation of a sensor static transfer function were proposed and classified into three major groups: analog, digital, and mixed-mode [5], [6]. The classification is based on whether the linearization is performed before, after, or during analog-to-digital (A/D) conversion of the sensor output signal.

Analog methods are based on analog signal processing using active or passive electronic components and circuits, such as bridge circuits [3], [6]-[8], a voltage divider [3], [9], a logarithmic amplifier [6], or an amplifier with positive feedback [10], [11]. The analog circuits can be very effective in narrow temperature ranges and represent low-cost and low-power solutions. However, analog linearization methods are sensitive to environmental factors, need to be adjusted for a specific sensor, and are used only when the output signal is required in analog form.

Digital methods perform linearization of a sensor output signal after it is converted into the digital form. One of the most frequently used methods from this group is the application of a look-up table stored in a ROM memory [6]. Also, there are measurement systems where a microcontroller or a microcomputer is used, so its processing power can be exploited for sensor linearization [12], [13]. An additional possibility is the application of an artificial neural network for sensor nonlinearity reduction in embedded systems based on microcontrollers [6], [14], [15]. To summarize, digital

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linearization methods are more flexible and provide the required measurement accuracy. However, these benefits come with several drawbacks, such as high occupancy of silicon area and long processing time, which are undesirable for low-cost and low-power applications.

Finally, methods from the mixed-mode group are known for simultaneous sensor linearization and A/D conversion of the sensor output signal. For this purpose are used special, nonlinear analog-to-digital converters (ADCs) with a transfer (quantization) function that is an approximation of a function inverse to the sensor transfer function [16]-[19]. In this manner, two signal processing steps are performed at the same time and by the same circuit, which is cost-effective in terms of power consumption, processing time, and production costs.

In this paper, the mixed-mode method based on a cost-effective dual-stage piecewise linear ADC design is proposed and used for the Pt100 sensor linearization. The proposed method is tested in three temperature ranges: 1) between - 200 °C and 850 °C, 2) between 0 °C and 500 °C, and 3) between -50 °C and 150 °C. The comparison between maximal absolute nonlinearity error and relative nonlinearity error before and after linearization will provide the efficiency assessment of the proposed method in Pt100 nonlinearity reduction.

2. PT100 STATIC TRANSFER FUNCTION

The relationship between resistance and temperature of a PRTD sensor over the whole measurement range, also called the static transfer function, can be described with the Callendar-Van Dusen polynomial equation widely used in the IEC 60751:2008 standard [1], [20]. For temperatures below 0 °C, the third-order polynomial equation is used:

$$R_S(T) = R_0 \cdot \left(1 + A \cdot T + B \cdot T^2 + C \cdot T^3 \cdot (T - 100)\right), \quad (1)$$

while for temperatures above 0 °C, PRTD resistance can be determined using the second-order polynomial:

$$R_S(T) = R_0 \cdot \left(1 + A \cdot T + B \cdot T^2\right), \quad (2)$$

where $R_S[\Omega]$ is the sensor resistance at temperature $T[°C]$, and $R_0[\Omega]$ is the sensor resistance at $T = 0$ °C. The values of coefficients used in (1) and (2) are defined with the IEC 60751: 2008 standard: $A = 3.9083 \cdot 10^{-3}[°C^{-1}]$, $B = -5.775 \cdot 10^{-7}[°C^{-2}]$ and $C = -4.183 \cdot 10^{-12}[°C^{-4}]$ [20]. Fig.1. presents the static transfer function and the absolute nonlinearity error variation throughout the measurement range for the Pt100 sensor (PRTD with $R_0 = 100\ \Omega$). From Fig.1., it is observable that in the given measurement range, maximal absolute nonlinearity error $\Delta T_{max}[°C]$ equals 46.3617 °C. Relative nonlinearity error $NE_T[\%]$ can be calculated as follows:

$$NE_T[\%] = \frac{\Delta T_{max}}{FS} \cdot 100\%, \quad (3)$$

where $FS[°C]$ represents the width of the measurement range. The values of $\Delta T_{max}[°C]$ and $NE_T[\%]$ for three temperature ranges are given in Table 1.

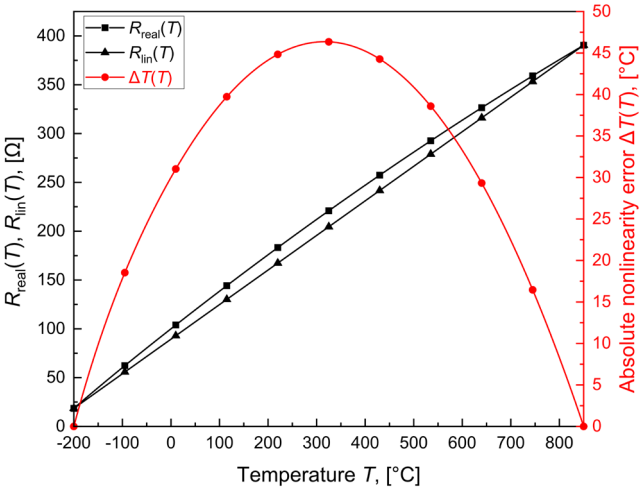


Fig.1. Static transfer function $R_{real}(T)$, linear end-point fit $R_{lin}(T)$, and absolute nonlinearity error $\Delta T(T)$ for Pt100 sensor.

Table 1. Maximal absolute nonlinearity error ΔT_{max} and relative nonlinearity error NE_T of a Pt100 sensor before linearization for three temperature ranges.

Temperature range	Type of error	Before linearization
-200 °C – 850 °C	$\Delta T_{max}[°C]$	46.3617
	$NE_T[\%]$	4.42
0 °C – 500 °C	$\Delta T_{max}[°C]$	9.9712
	$NE_T[\%]$	1.99
-50 °C – 150 °C	$\Delta T_{max}[°C]$	1.5099
	$NE_T[\%]$	0.755

3. PT100 INTERFACING CIRCUIT

In the proposed configuration, a Pt100 sensor is connected to an interfacing circuit using four lead wires, where two wires are connected to each side of the sensor (see Fig.2.). In this manner, the Pt100 sensor excitation current flows through one wire on each side (excitation wires L1 and L4), while the voltage generated on the Pt100 sensor is measured on the other two wires (sense wires L2 and L3). In this arrangement, the generated voltage is not affected by the reaction of the lead wire resistance with the excitation current. In other words, the circuit shown in Fig.2. takes advantage of the 4-wire configuration, which provides the most accurate measurements [10], [11], [21]-[23].

For choosing the most suitable PRTD and excitation current value, a balance between resolution and response time needs to be provided. Low resistance PRTD provides a shorter response time. However, to maintain the same voltage on the PRTD resistance and high resolution, a higher excitation current is needed. On the other hand, a higher excitation current increases the self-heating of the PRTD, which introduces error in the measured temperature by raising the sensor temperature above the measured object temperature. Very often, the excitation current for a Pt100 sensor has a value of 1 mA [24]. In this paper, the excitation current of 1 mA is provided with a constant current source consisting of a 2.5 V voltage reference, a precision amplifier, and a resistor $R_1 = 2.5$ kΩ (see Fig.2.) [23].

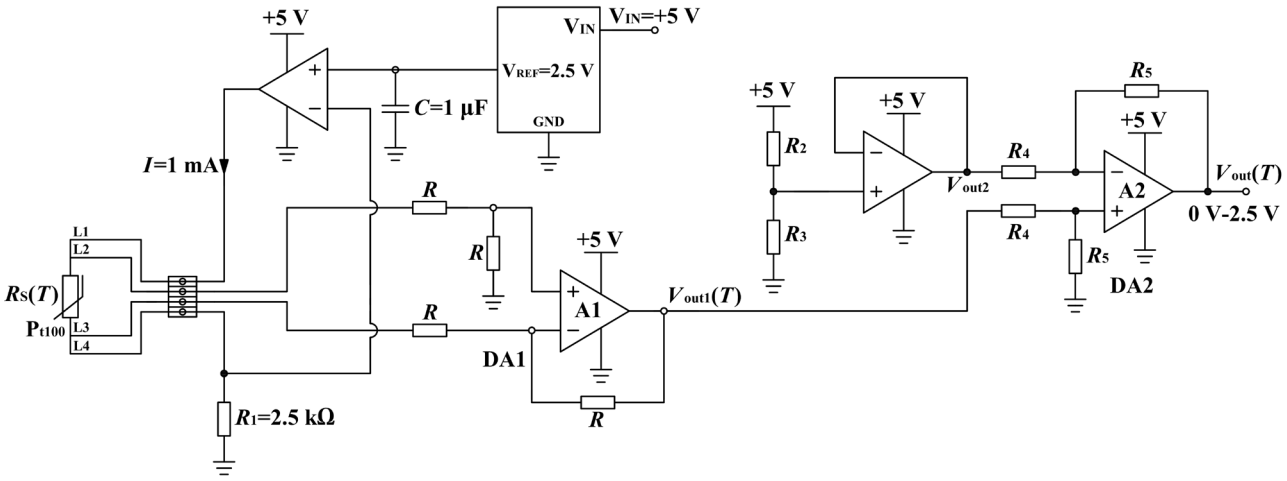


Fig.2. Pt100 interfacing circuit.

Table 2. The numerical values of the interfacing circuit components for three temperature ranges.

Temperature range	R_2	R_3	R_4	R_5	**A2**
-200 °C – 850 °C	10.2 kΩ	37.9 Ω	1.8 kΩ‖220 kΩ	12 kΩ	6.721212
0 °C – 500 °C	10.2 kΩ	208 Ω	10.2 kΩ+953 Ω	154 kΩ	13.807944
-50 °C – 150 °C	2.91 kΩ	47.5 kΩ	11.8 kΩ‖324 MΩ	383 kΩ	32.458676

The next segment of the interfacing circuit is a unity-gain differential amplifier DA1 which provides an output voltage $V_{out1}(T)$ nonlinearly dependent on the measured temperature. The rest of the interfacing circuit adjusts the output voltage $V_{out}(T)$ between 0 V and 2.5 V for each of the three considered temperature ranges. In this manner, the same linearizing ADC, with a 2.5 V input range, can be used for linearization in three temperature ranges.

The adjustment of the lowest output voltage $V_{out}(T_{min})$ to 0 V is performed by subtracting a voltage $V_{out2} = V_{out1}(T_{min})$ from a voltage $V_{out1}(T)$. The voltage V_{out2} is obtained using a voltage divider composed of resistors R_2 and R_3. The following unity-gain non-inverting amplifier is used only for the impedance adjustment. Voltages $V_{out1}(T)$ and V_{out2} are brought to inputs of a differential amplifier DA2 with a gain factor A2 calculated as follows:

$$\mathrm{A2} = \frac{2.5\mathrm{V}}{V_{\mathrm{out1}}\left(T\right)_{\max} - V_{\mathrm{out2}}} = \frac{R_5}{R_4}, \tag{4}$$

where $V_{out1}(T)_{max} = V_{out1}(T_{max})$ (since $V_{out1}(T)$ is a monotonically rising function). Resistors R_4 and R_5, from DA2, are selected to provide the specific value of A2 (see (4)), i.e., to set the output voltage $V_{out}(T_{max})$ to 2.5 V. The values of resistors R_2, R_3, R_4, and R_5, and the gain factor A2 are given in Table 2. for three temperature ranges. The resistor values are chosen according to the IEC 60063:2015 standard [25]. The following figure shows the output voltage $V_{out}(T)$ for three temperature ranges.

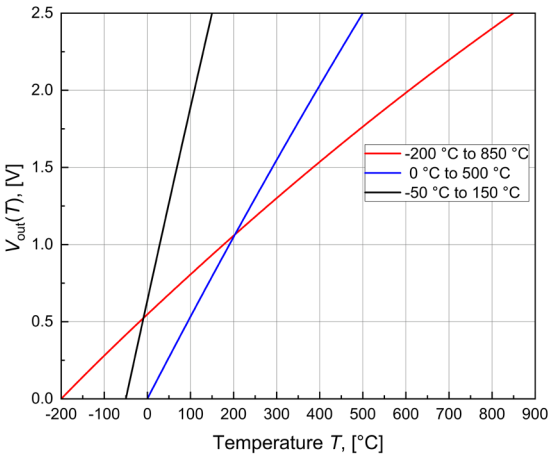


Fig.3. Interfacing circuit output voltage.

4. PROPOSED DESIGN OF A MIXED-MODE LINEARIZING CIRCUIT

The proposed mixed-mode linearization method is based on a compact design of a dual-stage piecewise linear ADC (dual-stage PWL ADC) [6], [9], [16]-[19], [26], [27]. The first stage is performed by an ADC based on a flash architecture with a novel sequential design, while the second stage is performed with a 24-bit delta-sigma ADC with a differential input and differential reference [28]. The role of the first stage flash ADC is to perform the linearization of a nonlinear voltage brought to its input (voltage $V_{out}(T)$, from Fig.3.). For this goal, a transfer function (quantization function) of the

proposed flash ADC is programmed to be the PWL approximation of a function inverse to the voltage $V_{out}(T)$. In other words, the ADC transfer function consists of nonuniform, i.e. differently wide linear segments bounded by break voltages [6], [9], [16]-[19], [26], [27]. The transfer function of the dual-stage PWL ADC is shown in Fig.4.

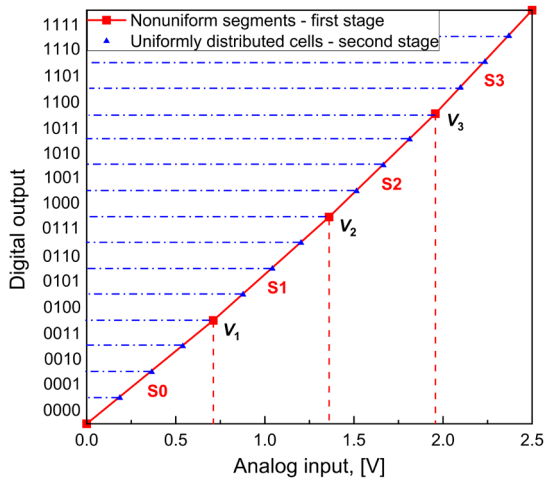


Fig.4. A dual-stage PWL ADC transfer function with corresponding break voltages and cell boundaries ($N_1 = N_2 = 2$ bits).

For easier understanding, Fig.4. shows the case where both stages have the same 2-bit resolution ($N_1 = N_2 = 2$ bits, where N_1 and N_2 represent the first and the second stage resolution, respectively). In this case, there are four nonuniform linear segments S_j, $j = 0,\ldots, 2^{N1}$-1 (red lines bounded by red dots as break voltages), and four uniformly distributed cells per segment (bounded by blue dots). The segments are different in width (S0 is the widest), and the cells from different segments differ by width as well. The break voltages V_i, $i = 1,\ldots,2^{N1}$-1 are determined in the following manner: 1) the temperature range of the function $V_{out}(T)$ from Fig.3. is divided into 2^{N1} equally wide segments, and 2) the segment boundaries are projected on the voltage axes of the $V_{out}(T)$ function. In other words, break voltages are calculated as follows:

$$V_i = V_{\text{out}}\left(T_i\right), i = 1,\ldots,2^{N_1} - 1, \tag{5}$$

where T_i is determined as below:

$$T_i = T_{\min} + i \cdot \frac{T_{\max} - T_{\min}}{2^{N_1}}, i = 1,\ldots, 2^{N_1} - 1. \tag{6}$$

Temperatures T_{min} and T_{max} represent the lowest and the highest temperature in the observed temperature range, respectively. In a real circuit, the break voltages are set by trimming resistors of a resistive ladder network with reference voltage set to $V_{REF} = V_{max} = V_{out}(T_{max})$.

The role of the second conversion stage is the determination of a uniform cell to which the current input sample belongs. The cell boundaries V_{jk} are determined in the following manner:

$$V_{jk} = V_{j1} + k \cdot \frac{V_{j\text{h}} - V_{j1}}{2^{N_2}}, j = 0,\ldots,2^{N_1} - 1, k = 1,\ldots,2^{N_2} - 1, \tag{7}$$

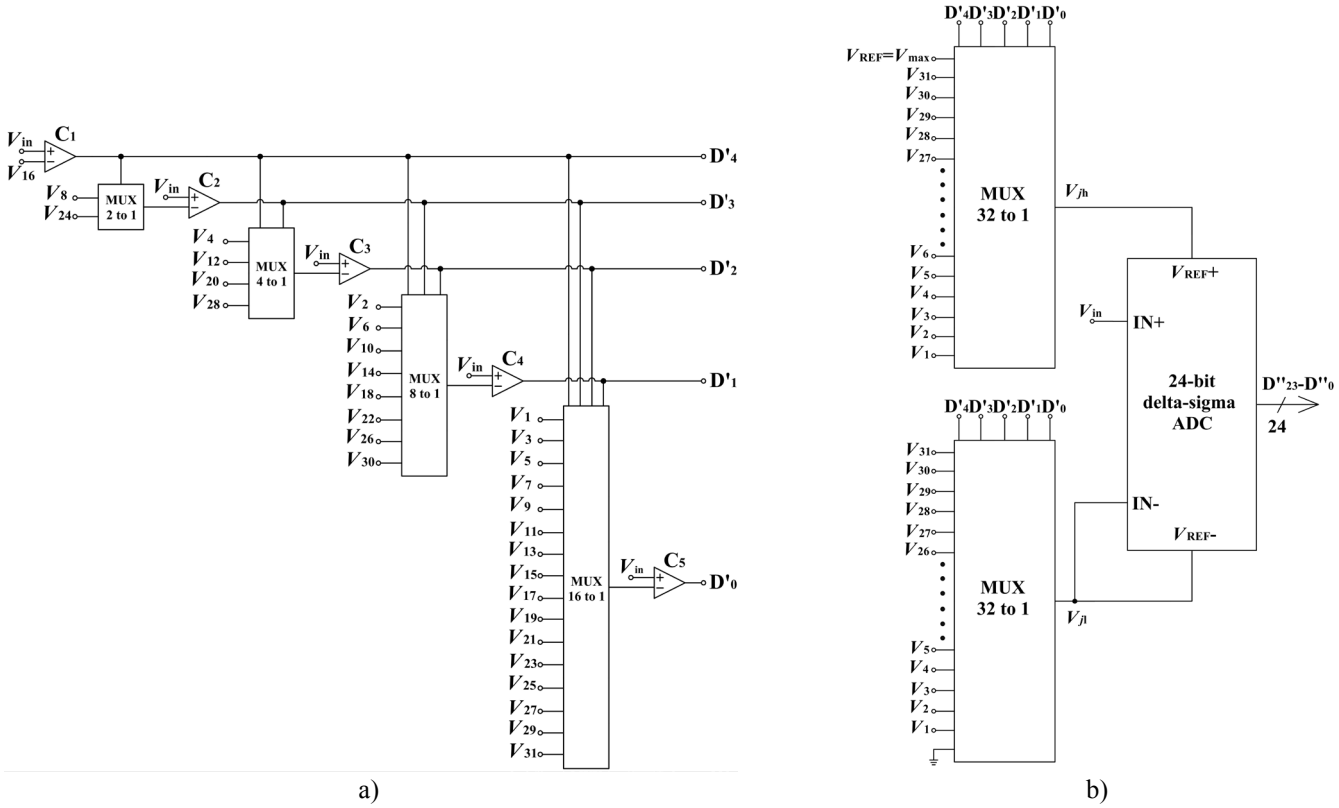
where j is the segment ordinal number, k is the cell boundary ordinal number within the j-th segment, and V_{j1} and $V_{j\text{h}}$ are the lower and higher boundary of the j-th segment, respectively.

The first stage of the proposed mixed-mode circuit is shown in Fig.5.a). The idea for using a novel sequential flash ADC design came from the need to achieve the same ADC resolution with a smaller number of employed comparators. A comparator is a great consumer of power and PCB area, which is unacceptable for low-power and low-cost applications. There are different methods to reduce the number of employed comparators in dual-stage PWL ADC design that were already proposed [26], [27]. However, the principle used in this paper is one of the most effective regarding this matter [29]. The reduction of comparator count is achieved by introducing analog multiplexers, while a priority encoder from the conventional flash ADC design is not needed [26]. Each analog multiplexer, controlled by digital outputs of previous comparators, determines the reference voltage for the next comparator in line. As a result, the proposed flash ADC architecture has a sequential design that demands a lower number of employed comparators than the conventional design of a flash ADC. In the proposed design, for the N_1-bit ADC, the number of used comparators is N_1, while for a flash ADC of the conventional design, 2^{N1}-1 comparators are needed.

The proposed sequential design of the flash ADC is similar to the pipeline ADC design since both perform operations over the input sample sequentially, i.e. in series. However, the goal to design a compact and low-cost ADC for Pt100 linearization is hardly achievable based on the pipeline ADC architecture since it is very complex [30]. Another reason why the pipeline ADC is not considered is that the flash architecture is more convenient for sensor linearization since the break voltages can be used as the reference voltages of the comparators, as in [6], [9], [17]-[19], [26], [27].

Fig.5.a) shows the case for $N_1 = 5$ bits where it can be easily observed that only five comparators are used (C1-C5), while 31 reference voltages (V_1-V_{31}) are still needed. As a result of the conversion, a 5-bit digital code is obtained (D'_4-D'_0) representing the segment to which the current input sample V_{in} belongs. The same bits (D'_4-D'_0) control the outputs of two 32 to 1 analog multiplexers, which are put between two conversion stages to select voltages V_{j1} and $V_{j\text{h}}$ (see Fig.5.b)). These voltages define the input range of the 24-bit delta-sigma ADC from the second stage of conversion [28]. A 24-bit code (D''_{23}-D''_0) obtained by delta-sigma ADC represents the uniform cell to which the input sample belongs.

In the case of a Pt100 sensor, the high conversion speed is not of great importance since the temperature is a slowly varying physical quantity. However, high ADC resolution, especially in the second stage of conversion, is essential for reducing the quantization error introduced in the first stage and for minimizing the quantization error generated during the second stage. For this purpose, delta-sigma ADC, known for high resolution and low conversion speed, is used.



a) b)

Fig.5. a) Sequential design of the first stage flash ADC, b) Determination of the input range for the second stage ADC.

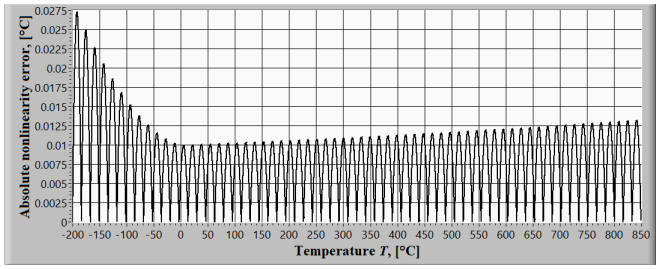
5. RESULTS AND DISCUSSIONS

The numerical results used to assess the proposed method efficiency in Pt100 nonlinearity compensation are derived using the simulation program LabVIEW. A virtual instrument (VI) is created to simulate the working principle of the measurement system consisting of the Pt100 sensor, the interfacing circuit and the proposed dual-stage PWL ADC. Within the main VI, the simulations of the Pt100 sensor and the interfacing circuit (see Fig.2.) are performed with a special subVI. Specifically, the subVI simulates the Pt100 transfer function $R_S(T)$ (according to (1)), generates the voltages $V_{out1}(T)$ and V_{out2}, subtracts them and multiplies their difference with the gain factor A2. In this manner voltage $V_{out}(T)$ is obtained (shown in Fig.3.). Another section of the VI is devoted to the calculation of break voltages according to equations (5) and (6). The first stage of conversion is performed by comparing the current input sample of the voltage $V_{out}(T)$ with the break voltages. In this manner, the ordinal number of the segment is determined (N_1 output bits are generated), and then its boundaries are selected from the set of break voltages. Then, the second stage of conversion follows. In this stage, the uniform cell to which the input sample belongs is determined and the N_2-bit digital code is obtained. This procedure is repeated for each sample of the input voltage $V_{out}(T)$. Digital codes from both conversion stages are combined and converted back to analog form, i.e. the measured value of the temperature is determined. Measured temperature values are compared to the real temperature values and the errors are calculated. The values of maximal absolute nonlinearity error ΔT_{max} and relative nonlinearity error NE_T are derived for three temperature ranges and three different values of N_1 (4, 5, and 6 bits). The resolution of the second stage is 24 bits in all cases (see Table 3.).

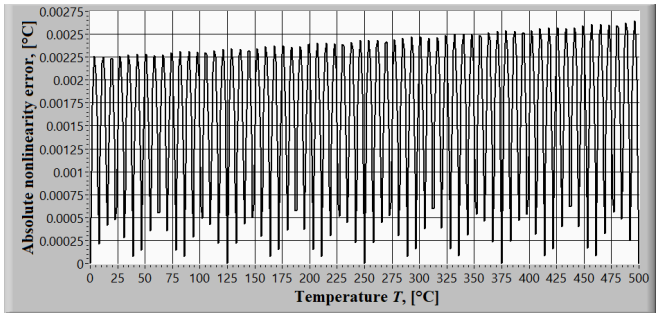
By observing the results given in Table 3., one can conclude that higher resolution in the first, i.e. linearizing stage, results in lower nonlinearity errors for all temperature ranges. In other words, the greatest impact on the nonlinearity error reduction has the 6-bit flash ADC, while the 24-bit ADC from the second stage reduces the quantization error generated during the first stage of conversion (5th column in Table 3.). Therefore, the second stage of conversion has a smaller impact on the measurement accuracy improvement. On the other hand, the increase of the resolution N_1 would significantly improve the measurement accuracy, but would also increase the number of break voltages that need to be calculated. For previous reasons, the resolution of $N_1 = 6$ bits is chosen as optimal, i.e. its value represents a compromise between nonlinearity error reduction rate and the complexity of break voltages calculation. Also, the errors are lower for narrower temperature ranges, which is of great importance for some applications. Noteworthy is that the obtained nonlinearity errors include the PWL approximation error generated during the calculation of break voltages. It was aimed to calculate the break voltages as simply as possible and without the need for a processor. For this aim, the break voltages are determined without limiting the PWL approximation error to some predefined value.

Table 3. Maximal absolute nonlinearity error ΔT_{max} and relative nonlinearity error NE_T of a Pt100 sensor after linearization for three temperature ranges.

Temperature range	**Type of error**	**After linearization**			
		N_1=4 bits, N_2=24 bits	**N_1=5 bits, N_2=24 bits**	**N_1=6 bits, N_2=24 bits**	**Error reduction rate in the best case (N_1=6 bits)**
-200 °C – 850 °C	**ΔT_{max}[°C]**	0.3816	0.1044	$2.73 \cdot 10^{-2}$	1698
	NE_T[%]	$3.63 \cdot 10^{-2}$	$9.9 \cdot 10^{-3}$	$2.6 \cdot 10^{-3}$	1700
0 °C – 500 °C	**ΔT_{max}[°C]**	$4.21 \cdot 10^{-2}$	$1.05 \cdot 10^{-2}$	$2.6 \cdot 10^{-3}$	3835
	NE_T[%]	$8.4 \cdot 10^{-3}$	$2.1 \cdot 10^{-3}$	$5 \cdot 10^{-4}$	3980
-50 °C – 150 °C	**ΔT_{max}[°C]**	$6.7 \cdot 10^{-3}$	$1.7 \cdot 10^{-3}$	$4.3 \cdot 10^{-4}$	3511
	NE_T[%]	$3.4 \cdot 10^{-3}$	$8 \cdot 10^{-4}$	$2.15 \cdot 10^{-4}$	3512



a)



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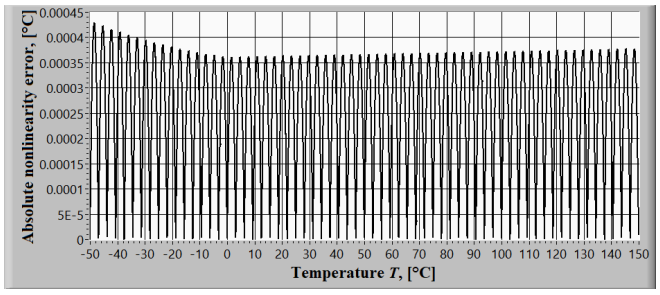

c)

Fig.6. Absolute nonlinearity error diagrams for three temperature ranges when $N_1 = 6$ bits and $N_2 = 24$ bits:
a) range between -200 °C and 850 °C, b) range between 0 °C and 500 °C, c) range between -50 °C and 150 °C.

For example, in the range between -200 °C and 850 °C, the errors after linearization are nearly 1700 times lower than the errors before linearization (error reduction rate given in Table 3). In the range between 0 °C and 500 °C, the error reduction rate is around 3900, and finally, in the range between -50 °C and 150 °C, the error reduction rate is around 3500. These results confirm a significant improvement in the temperature measurement accuracy.

Additionally, the variation of the absolute nonlinearity error throughout the measurement range is given in Fig.6. for three temperature ranges and the case when $N_1 = 6$ bits. The absolute error diagrams are drawn for 10000 points in each temperature range. Also, the shapes of error functions are independent of resolution N_1. In other words, regardless of the N_1 value, the absolute nonlinearity error will be higher for temperatures below 0 °C and with the temperature increase it will rapidly drop, around 0 °C it will have the lowest value, and after that point, it will slowly increase again. The previous conclusions explain why the error reduction rate is the highest for the range between 0 °C and 500 °C. However, the resolution N_1 affects the value of the maximal absolute nonlinearity error in each range, as can be noticed from Table 3.

To better understand the significance of the obtained results, they are compared to the best result achieved using the analog linearization method based on the bridge circuit proposed in [6]. The maximal absolute nonlinearity error obtained in [6] is 0.1 °C for the temperature range between 0 °C and 800 °C. In this paper, a wider range, between -200 °C and 850 °C, is examined, and the result from [6] is better only compared to the case when $N_1 = 4$ bits. However, the mixed-mode methods imply simultaneous linearization and analog-to-digital conversion using the same circuit. For this exact reason, the proposed mixed-mode method is characterized by shorter overall signal processing time, lower circuit complexity, lower production costs and lower power consumption when compared to an analog linearization circuit followed by an ADC, or an ADC followed by a digital linearization circuit. Another advantage of the proposed mixed-mode method is that it digitizes a sensor signal before its transmission, and it is known that digital transmission is less affected by interference and noise. Additionally, the first stage flash ADC is low-complex and low-power consuming even for high resolutions since the comparator count equals the ADC resolution.

6. CONCLUSION

A novel mixed-mode method, designed for a Pt100 sensor nonlinearity compensation has been proposed in this paper. The proposed method is based on the application of a newly developed dual-stage PWL ADC. The specificity of the proposed linearizing dual-stage PWL ADC represents the design of its first stage. The first stage of simultaneous A/D

conversion and linearization has been performed with a low-cost, low-power, and low-complex flash ADC of a novel sequential design. These attributes have been obtained by reducing the number of power-consuming components, such as comparators. The number of employed comparators is equal to the flash ADC resolution, which is a significantly lower number compared to the conventional flash ADC design. The second stage of conversion is performed using the 24-bit delta-sigma ADC with a differential input and differential reference.

Another significant contribution of this work is the high accuracy of temperature measurement, which has been achieved for three different temperature ranges: 1) between -200 °C and 850 °C, 2) between 0 °C to 500 °C, and 3) between -50 °C and 150 °C. The absolute and relative nonlinearity errors before linearization have been compared with the corresponding values after linearization. The conducted conclusions have undoubtedly proved the efficiency of the proposed linearization method. For example, in the widest temperature range, the relative nonlinearity error has been reduced from 4.42 % to $2.6 \cdot 10^{-3}$ %. In that case, the 6-bit flash ADC of the proposed sequential design and the 24-bit delta-sigma ADC have been used. For the narrower temperature ranges, nonlinearity errors have been even lower.

The proposed mixed-mode method is a low-cost, low-power, and high-efficiecy method for nonlinearity error reduction. It can be used for Pt100 sensors and other sensors with nonlinear and monotonically rising static transfer functions.

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