Estimation of Exponential ADC Test Signal Using Histogram

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Abstract. *The paper presents a new approach to the ADC INL testing methodology by simple monotonic exponential stimulus which data processing algorithm was suggested with targeting simple implementation in ADC on-board self-testing systems. The novelty of the approach is in determination of stimulus parameters by processing of real measured histogram of record instead of direct record processing in time domain that was used in previous papers. The method was verified by simulations and experimental measurements in comparison with standardised sinewave histogram test that confirmed applicability of the method.*

Keywords: Exponential Stimulus, Histogram Test, On-board ADC Testing

1. Introduction

Analogue-to-digital convertors (ADC) are the main hardware signal processing blocks performing quantization of analogue signals to digital representation (code k) within signal digitizing. Quantization levels of ADC (transient levels T_k) are expressed by ADC transfer characteristics. Generally the ideal ADC should have quantization levels uniformly distributed within ADC input range with constant difference between the neighbouring ones. This required difference is usually called nominal quantisation step Q (code bin width W_k). Unfortunately the real ADC have the transient level T_k distributed non-uniformly, i.e. code bin widths are not constant within the ADC full input range. Difference between nominal (ideal) T_k and real T_k or Q and W_k represents errors of real ADC transfer characteristics and usually it is described by so-called integral (INL) or differential nonlinearity (DNL) respectively (IEEE standards). Although the definition of DNL and INL is very simple the measurement of these error parameters is very complex task because of stochastically behaviour or real ADCs. It means that code k on the ADC output may stochastically change within a few neighbouring codes even if a DC signal is on ADC input. The most common methods for ADC testing eliminating the ADC stochastic behaviour is histogram method: the real histogram is built from record acquired on ADC output at known in details ADC input stimulus and this is post compared with theoretical histogram calculated for ideal equivalent ADC for the same stimulus. This method is standardised for sinewave stimulus. Because of required extreme quality of sinewave stimulus the generators suitable for testing 16 and more bits ADCs are rather expensive and less common in laboratories. To avoid this constraint other stimulus signals have been proposed for histogram tests [1], [2], [3], et al. Exponential stimulus seems to be one of the best alternative solutions because of its easy generation in on-board ADC self test system (see Fig. 1) ([4]).
The novelty of our approach presented in this paper is determination of stimulus parameters needed for modelling of histogram of ideal equivalent ADC (required for INL estimation) by processing of real measured histogram instead of stimulus record fitting that was used in previous papers ([5], [7]).

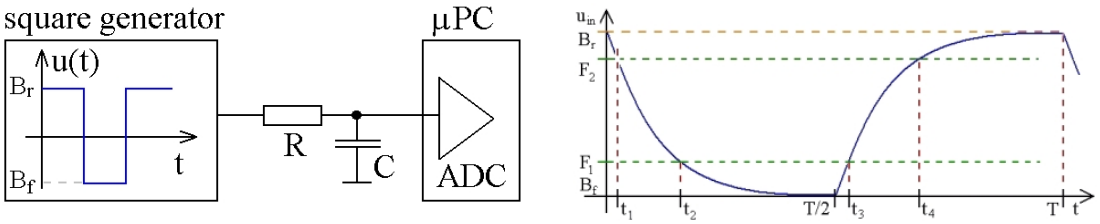

Fig. 1. Application of exponential stimulus in on-board system (left) and shape of exponential signal in time domain (right).

Mathematical representation of such a stimulus is as follows:

$$y(t)=\begin{cases}(F_2-B_f)\cdot e^{-\frac{t-t_1}{\tau_1}}+B_f, & for \quad (t_1<t<t_2)\\ B_r-(B_r-F_1)\cdot e^{-\frac{t-t_3}{\tau_2}}, & for \quad (t_3<t<t_4)\end{cases}. \tag{1}$$

where τ is the time constant of exponential pulse, F_1 and F_2 determines full-scale input range of ADC under test and B_f, B_r are limit values of exponential signal for t → ∞ for each direction (falling and rising) of signal.

2. Exponential stimulus histogram processing

The main goal of processing of measured histogram $H_m(k)$ is to estimate INL of ADC under test. The histogram can be achieved by processing either rising or falling part of stimulus in record. The expressions herein below describe INL estimation for any chosen slope.

To decrease calculation load, the INL can be calculated from recurrent expression:

$$INL(k+1)=INL(k)+DNL(k), \tag{2}$$

Where

$$DNL(k)=\frac{H_C(k)-H_{C_{id}}(k,B)}{H_{id}(k,B)}, \text{ for } k=1, 2, ..., 2^N-2, \tag{3}$$

N is number of bits of ADC under test, INL for the first and last transient level is equal zero, i.e. INL(1) = INL(2^N-1) = 0, $H_C(k)$ is cumulated normalized measured histogram:

$$H_C(k)=\frac{\sum_{i=1}^{k}H_m(i)}{\sum_{i=1}^{2^N-2}H_m(i)}=\frac{H_{mC}(k)}{H_{mC}(2^N-2)}=\frac{H_{mC}(k-1)+H_m(k)}{H_{mC}(2^N-2)}, \text{ for } k=2, 3, ..., 2^N-2, \tag{4}$$

and $H_{id}(k, B)$ is normalised histogram for ideal equivalent ADC. To build $H_{id}(k, B)$ only parameter B has to be estimated. Three formal mathematical expressions of $H_{id}(k, B)$ was published [4] in the past with the goal to simplify determination of B. The recurrent one was chosen to be applied in following because of its mathematical simplicity and using only basic arithmetic operations what is important in on-chip implementation.

The ideal histogram may be expressed ([4]):

$$H_{id}(k,B)=M(B)\cdot\frac{1}{F_1-B+Q\cdot(k-0.5)}, \text{ for } k=1, 2, ..., 2^N-2, \tag{5}$$

where

$$M(B)=\frac{1}{\sum_{i=1}^{2^N-2}\frac{1}{F_1-B+Q\cdot(i-0.5)}}, \tag{6}$$

and Q is nominal code bin width $Q=\frac{F_2-F_1}{2^N-1}$. The value $M(B)$ is independent of k and that is why it can be calculated only once for all values k in $H_{id}(k,B)$.

In general the simple histogram $H_{id}(k,B)$ is very sensitive on superimposed noise and harmonic disturbances in stimulus. That's why the normalized cumulative $H_{Cid}(k,B)$ is preferred for INL estimation:

$$H_{Cid}(k+1,B) = H_{Cid}(k,B) + H_{id}(k+1,B),\ H_{Cid}(1,B) = H_{id}(1,B),\ k=1, 2, \ldots 2^N-3. \quad (7)$$

3. Iteration algorithm for INL estimation

The both histograms $H_{id}(k, B)$ and $H_{Cid}(k, B)$ dependent only on parameter B is required to determine INL of ADC under test. In other words the only parameter that has to be estimated from measured histogram is parameter B. In praxis it can be estimated only numerically because the least mean square fit (LMS) (8) leads to a nonlinear equation that can not be solved analytically.

$$\min(\phi(B)) = \min\left(\sum_{i=1}^{2^N-2} \left(\hat{H}_C(i) - H_{C_{id}}(i,B) \right)^2 \right), \quad (8)$$

Where $\phi(B)$ is the cost function of LMS fit. Newton iteration algorithm can be applied to determine B from (8):

$$B_{n+1} = B_n - \frac{\phi'(B_n)}{\phi''(B_n)}. \quad (9)$$

Where $\phi'(B_n)$ and $\phi''(B_n)$ are computed numerically as follows:

$$\phi'(B) = \frac{\phi(B+h) - \phi(B-h)}{2 \cdot h}, \quad \phi''(B) = \frac{\phi(B+h) - 2 \cdot \phi(B) + \phi(B-h)}{h^2}, \quad (10)$$

And h is a constant dependent on number of bits used for representation of numbers in test data processing system, e.g. for double representation (64 bits) the recommended value of h is 10^{-3} - 10^{-4}. The iteration final condition is $\varepsilon > |B_{n+1} - B_n|$, where ε is approximation residual uncertainty. The resulting B is consequentially applied for estimation of INL of ADC under test according the procedure described hereinabove in chapter 2.

4. Experimental results

The proposed algorithm was verified by simulated measurement on simulated ADC with nominal modelled INL. Fig. 2 shows the nominal INL and INL calculated from record on the output of the modelled simulated ADC under test by the suggested algorithm for ideal exponential stimulus.

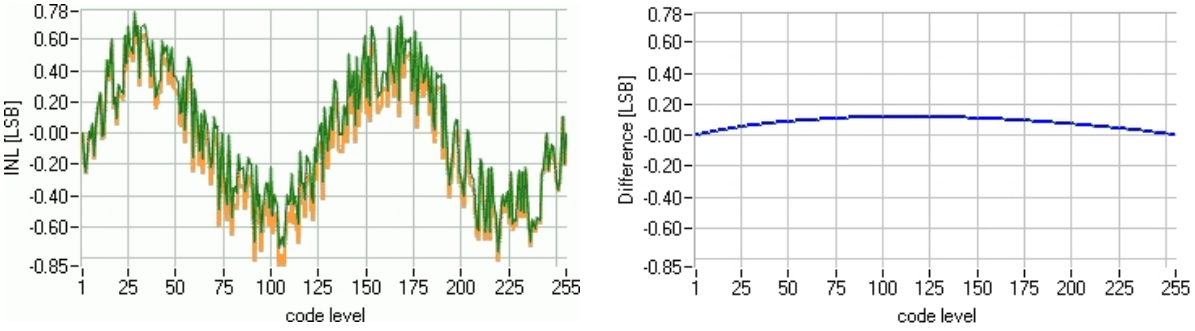

Fig. 2. The modelled (dark) and measured (light) INLs of simulated ADC (the left graph) and difference between them (the right graph).

As it can be seen from the figure there are only little differences between modelled and measured INL. The right graph shows differences of both INLs that can be supposed to be error of measurement.

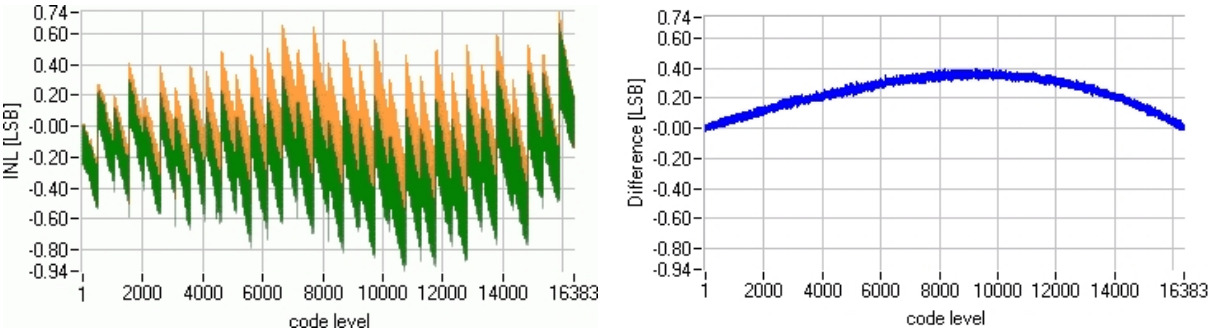

Fig. 3. INL of USB6009 obtained from standardized harmonic stimulus histogram test (dark) and from exponential stimulus histogram test (light) (left) and difference between them (right).

The proposed algorithm was also verified by real experimental measurement. The ADC under test was 14-bit ADC implemented in USB6009 device by National Instruments. The ADC was tested by standardized histogram test method with harmonic stimulus was used (dark curve in Fig. 3 left) as well as by algorithm described hereinabove (light curve in Fig. 3 left). The difference of INLs was calculated and it is shown in Fig. 3 (right).

5. Conclusions

The paper presents a new approach to the ADC INL testing methodology by simple monotonic exponential stimulus which data processing algorithm was suggested with targeting simple implementation in ADC on-board self-testing systems. The method was verified by simulations and experimental measurements in comparison with standardised sinewave histogram test that confirmed applicability of the method. The residual error of measurement can be caused by INL low code frequency component masking [6] if it has nature similar to the shape of input exponential stimulus.

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