

Investigating of Digital to Analog Converter Using Program Designed in LabVIEW Environment

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***Abstract.** An application has been designed in the LabVIEW environment for computer simulation of the operation principle and testing of binary weighted digital to analog converter (DAC). The front panel contains graphical objects, permitting interactive communication with the user. The application permits performance virtual experiments thanks to the possibility of the modification of the DAC electronic circuit parameters. The application can be used both for education and for specific research purposes.*

Keywords: LabVIEW, DAC Modelling, DAC Simulation

1. Introduction

Presentation of the operation principle of digital-to-analog converter (DAC) and experimental study of its properties in the traditional way is time consuming and poses difficulties for the lecturers and students because of the need to present considerable amounts of information in the graphical form. To illustrate the problems related to the DAC operation, many schemes and characteristics describing relevant properties of the system are needed and have to be adapted for each new value of the parameters of the converter scheme. One solution of this problem is to use computer based educational tools for lecturers and students to be used either in lectures or laboratory classes. In particular, the LabVIEW environment [1] seems to be commonly used at the university level teaching process for realisation of specific programs for presentation of various didactic problems. Many authors have been interested in these subject areas and many applications dedicated to the simulation both of the analog to digital and digital to analog converters [2-4] and measuring paths employing different sensors have been published [5].

This paper presents the application designed in the LabVIEW environment for computer simulation of the operation principle and testing of DAC based on binary weighted resistors ladder with the summing amplifier.

2. Simulation and Investigation of the Properties of the Binary Weighted Digital-to-Analog Converter

The binary weighted DAC is based on the circuit with a network of parallel branches (the so called resistor ladder), one branch for each bit. Each branch contains a resistance weighted in proportion to the significance of the bit in the digital word. The resistor ladder cooperates with the current summing amplifier. This is one of the fastest conversion methods but for a large number of ADC bits there are problems with accuracy because too much precision is required for the ladder resistors for the most significant bits. This type of converter is usually limited to 8-bit resolution. Because both the architecture and principle operation of this ADC circuit are relatively simple, so this type of ADC is excellent for educational purposes. Fig. 1 presents the front panel of the designed application for the simulation of a binary weighted DAC and illustrates the principle of operation of this converter.

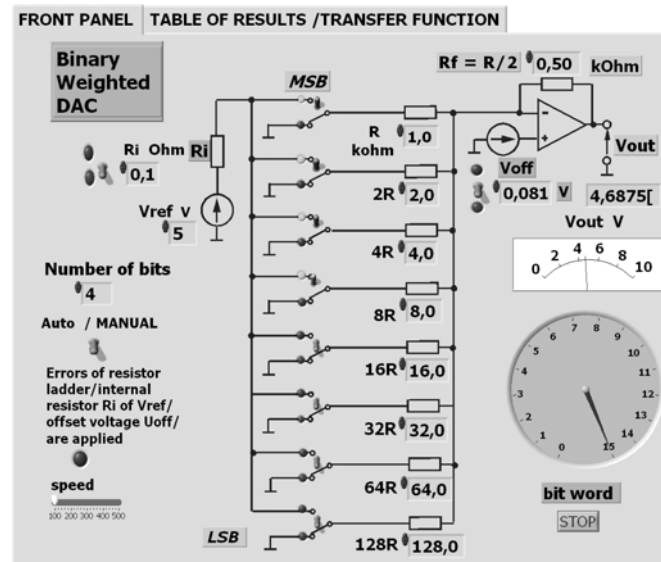


Fig. 1. The front panel of the designed LabVIEW application for the simulation of a binary weighted DAC

The output voltage value for the n-bits DAC is expressed as:

$$V_{out} = -V_{ref} \frac{R_F}{R} \left(\frac{1}{2^1} k_1 + \frac{1}{2^2} k_2 + \dots + \frac{1}{2^{n-1}} k_{n-1} + \frac{1}{2^n} k_n \right), \quad (1)$$

where V_{ref} is the reference voltage, k_n are individual bits of input word bits, R is value of the resistance in resistor ladder and R_F is a feedback resistor of the current summing amplifier. The front panel contains a block diagram of the DAC system and controls permitting preset of the desired values of the binary input signal or converter parameters and graphic displays at most important points of the system. The resolution from 2 bits to 6 bits of the DAC may be chosen by the computer operator by presetting a suitable number in the window “number of bits” of the application front panel. The results of simulation are presented in the second panel by using the bookmark “TABLE OF RESULTS/ TRANSFER FUNCTION” in form of plot of transfer function and the data are collected in the table of results.” Fig. 2 presents results of simulation 4-bits DAC for the ideal case - that is for the ideal values of DAC circuit parameters.

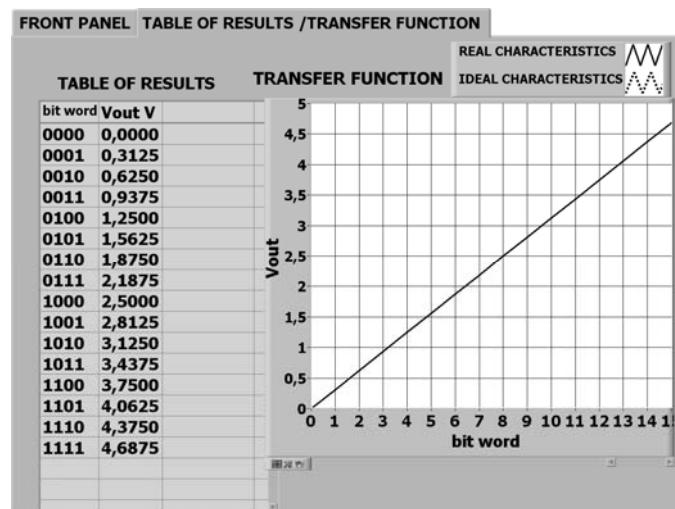


Fig. 2 The results of simulation of 4-bits DAC for the ideal case, all the DAC circuit parameters take the ideal values.

The application permits preset of all important parameters of the D/A circuit including: the reference voltage U_R , value of weighted resistor in each branch, feedback resistor R_F in current summing amplifier and offset voltage simulating the offset voltage of operational amplifier.

Fig. 3 presents the exemplary simulation for non-ideal parameters of DAC. The offset voltage $V_{off} = 0.2 \text{ V}$ is applied and the other DAC parameters are ideal. Fig. 4 presents the results of this simulation.

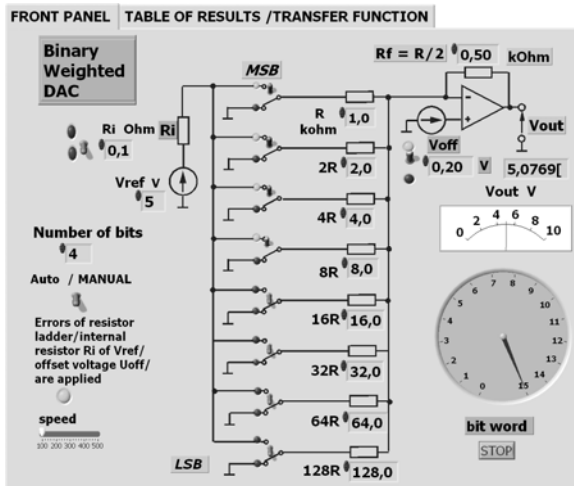


Fig. 3. The front panel for simulation of 4-bits DAC. The offset voltage value $V_{off} = 0.2 \text{ V}$. The other DAC parameters have ideal values.

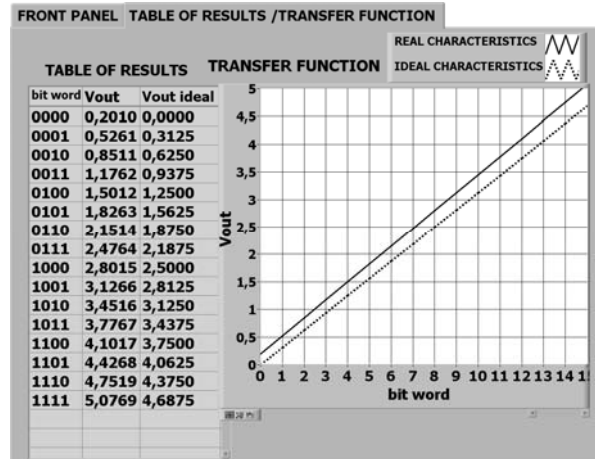


Fig. 4. The results of simulation of 4-bits DAC for the offset voltage value $V_{off} = 0.2 \text{ V}$. The other ADC parameters have ideal values.

The results of this investigation presented in Fig.4 show that both an offset error and a gain error of transfer function have occurred. As follows from the results of the simulation presented in Fig.4 (result tables and plot of transfer function), these errors have no effect on the linearity of the transfer function.

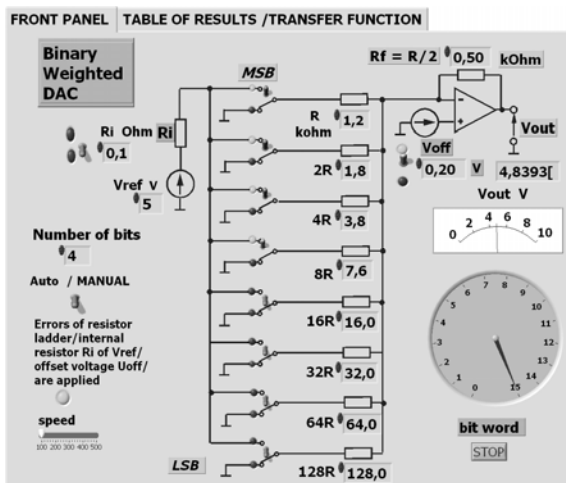


Fig. 5. The front panel for simulation of 4-bits DAC. The offset voltage value $V_{off} = 0.2 \text{ V}$. The values of ladder resistors are improper.

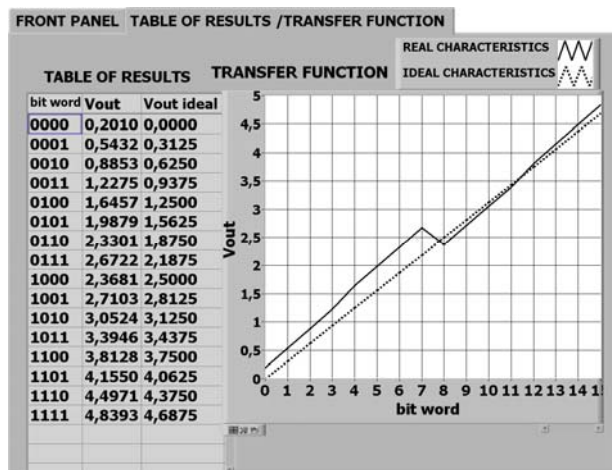


Fig. 6. The results of simulation of 4-bits DAC for the offset voltage value $V_{off} = 0.2 \text{ V}$ and for improper values of ladder resistors.

Fig. 5 presents results of another simulation for non-ideal parameters of DAC. The offset voltage $V_{off} = 0.2$ V is applied and the ladder resistors are preset on improper values. Fig. 6 presents the results of this simulation. The results of the simulation presented in Fig. 6 show that improper values of the ladders resistors cause non-linearity of the DAC transfer function and can additionally cause non-monotonicity of the transfer function. All data are collected in the table of results and can be exported to another program (an example Excel) for further data processing such as calculating of linearity errors, gain error, offset error etc.

3. Conclusions

The LabVIEW application written permits presentation of the principles of operation of the binary weighted digital-to-analog converter and performance of simulation experiments thanks to the possibility of preset of the parameters of the digital input signal and those of the elements of the converter system. Students can analyse the effect of changes in the parameters of the DAC system on the plot of transfer function shown in the second window of the front panel which is activated after switch of bookmark. All results of the simulation are collected in table of results and can be exported to another program for further processing. An important advantage of this application over similar ones presented in literature is the possibility of setting a large number of parameters of the system over wide ranges. The application permits performance of virtual experiments thanks to the possibility of modification of the DAC electronic circuit parameters. The application can be used both for education and for specific research purposes. The analysis of the converter work and the effects of different parameters on its performance is conducted in the interactive mode and can be realised with the help of a PC unit only, so the results are achieved very fast.

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