

Estimation of ADC Nonlinearities from the Measurement in Input Voltage Intervals

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Abstract. This paper present proposal for fast testing method of AD converters aimed for estimation of INL as the error function and superimposed uncertainty based on two dimensional ADC error model. INL function is being determined by curve fitting of approximation function from the measurement of $INL(k)$ in chosen code bins of the full scale range of ADC under test. Proposed testing method is suitable for approval of final accuracy of assembled data acquisition system.

Keywords: — Analog to Digital Converters (ADC), Curve Fitting, Integral Nonlinearity (INL), Error Function, Uncertainty

1. Introduction

This paper presents a simple experimental method of testing INL characteristics of AD converters which can be performed in laboratories of end user. Test method works with several code bins which are important to approximate of integral nonlinearity as a basic parameter describing deviation in the transfer characteristic.

Integral nonlinearity $INL(k)$ and average code bin width Q' are defined according to [1], [2]. Taking into account Terminal based definitions transient code levels idea and real at both ends are equal $T_{id}(0) = T(0)$ and $T_{id}(2N-1) = T(2N-1)$

The characteristic of a real AD converter could be described by the two dimensional model [1]. INL is being described by the formula

$$INL(k) = {}^{LCF}INL(k) + {}^{HCF}INL(k) \quad (3)$$

Where low code frequency component ${}^{LCF}INL$ represents smothered component of INL function while high code frequency component ${}^{HCF}INL$ describes deterministic and stochastic effects of ADC nonlinearities. There are various mathematical methods proposed in the literature which approximate ${}^{LCF}INL(k)$ with sufficient accuracy [4], [5]. The optimal type of approximating function depends on shape resulting error function conditioned by the ADC architecture and utilized technology.

From the metrological point of view, with increasing approximation order the ${}^{LCF}INL(k)$ convert to the systematic ADC error and remaining ${}^{HCF}INL(k)$ covers all remaining stochastic error sources. Impact of all those error sources could be described by combined uncertainty.

2. Curve fitting method for approximation of the INL characteristics

The proposed test method is based on the approximation of the ADC error characteristics by a polynomial.

$$INL(k) = a_m k^m + a_{m-1} k^{m-1} + \dots + a_1 k + a_0 \quad (4)$$

The parameters a_0, a_1, \dots, a_m , are estimated using the least mean square (LMS) criteria

$$E = \min \sum_{k=k_1}^{k_n} \left[\text{INL}(k) - (a_m k^m + a_{m-1} k^{m-1} \dots + a_1 k_1 + a_0) \right]^2 \quad (5)$$

The number n of codes ($k_1 \dots k_n$) where the integral nonlinearity $\text{INL}(k)$ have to be measured is lower than all ADC codes, which allows to speed up testing procedure. The transient code levels $T(k)$ in the L interleaved nodes (k_2, k_{n-1}) are measured by standardized testing method [3].

3. Uncertainties and Errors of Measuring of Code Bins

The INL measured in chosen code bins gives information just about systematic error. Uncertainty determines the margin of error of the tested error function by giving a range of values likely to enclose the true value. The combined uncertainty consists from following components in our case.

The first one u_1 represents the testing uncertainty caused by the utilized testing method. It belongs to the uncertainty of type A and could be determined by the repetition of measurement of code bins. We have used 10 measurement for any code bin k . Uncertainty $u_1(k)$ of transient code level testing determines uncertainty of $\text{INL}(k)$ in the nodal code bin.

$$u_1(k) = 3 \sqrt{\frac{1}{l(l-1)} \sum_{i=1}^l (T_i(k) - \overline{T(k)})^2} \quad (6)$$

The total uncertainty of INL estimation in the L nodal points is being determined by the geometrical sum. Uncertainty in nodes $k=0$ and $k=2^N-1$ are zero.

$$u_1 = \sqrt{\left(\frac{1}{L} \left[\sum_{i=1}^L u_1^2(i) + u_1(i) \sum_{\substack{j=1 \\ i \neq j}}^L u_1(j) r_{ij} \right] \right)} \quad (7)$$

where r_{ij} represents the cross correlation between testing results in any nodal point k_n .

The second uncertainty component is determined by the uncertainty of the precise digital voltmeter, which is responsible for traceability of measured code levels. This value could be estimated by the u_2 uncertainty of type B taken from the voltmeter data sheet.

The third component is connected with approximation uncertainty expressed by the approximation mean square error $u_3 = 3 \cdot Q \cdot \sqrt{E}$. This component has no correlation to the other uncertainty components. The uncertainty expressed in the codes must be transformed in voltage.

The total combined uncertainty of testing procedure u_c is being determined by all three contributions. No correlation between them is considered.

$$u_c = 3 \sqrt{\sum_{i=1}^3 u_i^2} \quad (8)$$

Combined uncertainty is an optimal indicator of test confidence. Determination of $\text{INL}(k)$ systematic error is reliable when final uncertainty is lower than maximal value INL_{max} . This figure of merit allows end user to improve its testing procedure in two directions.

The first one is based on the determination of bottlenecks in the proposed method by selection of uncertainty components contributing dominantly to the combined uncertainty. It allows enhancing number of testing attempts, improving the quality of reference voltmeter or increasing order of approximating polynomial.

The second possibility how to achieve satisfying ratio between u_c and INL_{max} is the enhancement of the amount of the testing nodes and order of the polynomial approximation.

Impossibility to achieve required limits of combined uncertainty is a sign that standardized methods has to be applied. As mentioned in paper [6] the suitable error models are dependent on ADC technology.

Besides converter error the digital results at the ADC output are always corrupted by the quantization noise which theoretical value is $u_q = \frac{Q}{\sqrt{12}}$. When the testing combined uncertainty and maximal value of error function are lower than quantization uncertainty it has no sense to perform correction using error function.

4. Experimental Results

Proposed method was tested by two types of ADCs each one representing another internal architecture. First one is 12 bit ADC of type TC7109 A by Microchip based on the double slope integration principle with autozeroing phase. Second tested ADC was 8-bit ADC0804 by Intersil working on the successive approximation principle.

The (Fig. 1.a.) shows results of approximation of the first ADC (TC 7109 A) by the polynomial of 5,10,3-th order when $L=20$ equidistant points in the transfer characteristic were taken for INL estimation. The integral nonlinearity by the standardized method is on (Fig.1.b).

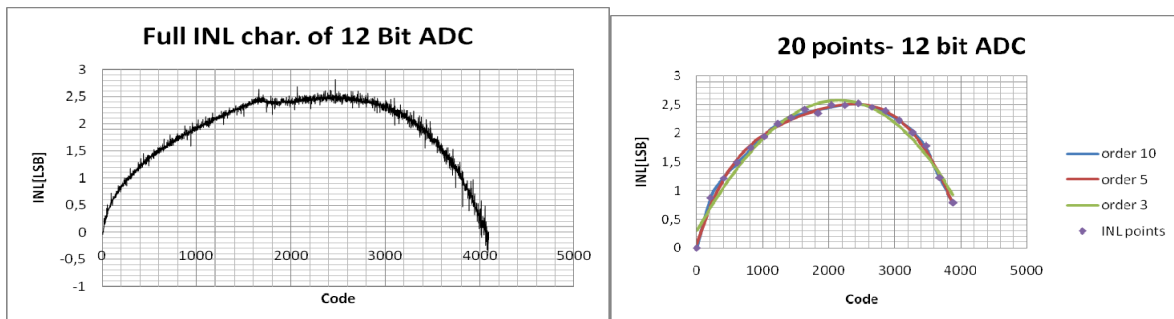


Fig.1a.) Fig. 1. Measured INL of TC7109 by standardized method b.) approximated function with polynomial of 3,5,10 th order for 20 nodes

The (Fig. 2a). shows results of approximation of ADC0804 with different order. The difference between approximated polynomial and real INL measured by standardized methods is shown on (Fig.2.b). Typical consequence of DAC in the feedback is periodical repetition of the characteristic values of INL over the full scale. The uncertainty components contributions and their impact on combined one are shown on (Tab.1).

Table 1. Final uncertainties for both ADCs with use variety of nodal points

Type of ADC	Nod. points	u_1 [μV]	u_2 [μV]	u_3 [μV]			u_c [μV] 10 pol.
				Order of pol.			
				10	5	3	
8 bit ADC – ADC0804	20	26,893	5,5	4041,87	6097,51	6421,92	12125
	30	19,855		4769,79	6301,83	6735,794	14309,5
	50	23,715		4988,11	6162,17	6423,92	14946,51
12 bit ADC- TC7109	20	18,582		150,517	312,473	671,036	455,27
	30	22,469		99,861	140,156	377,977	307,515
	50	22,404		142,232	176,975	385,502	432,272

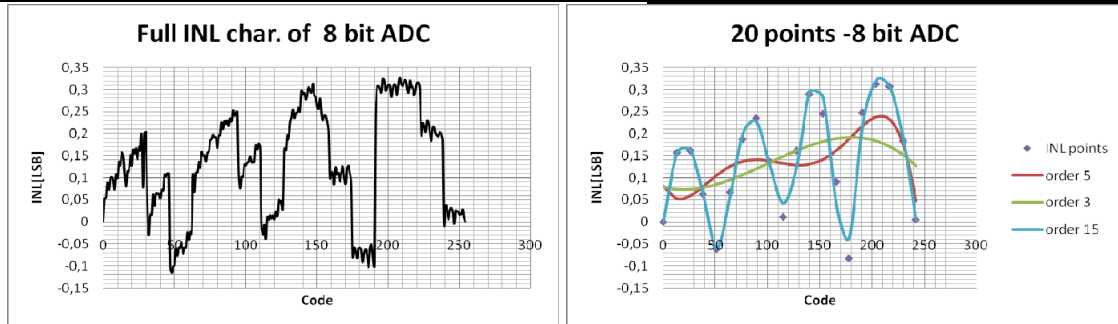


Fig.2a.). Measured INL of ADC0804 by standardized method b.) approximated function with polynomial of 3,5,10 th order for 20 nodes

Conclusions

Experimental results show that approximation of ADCs' INL by a polynomial function on the base of measurement in the reduce amount of measured points of its FSR is a suitable method which can speed up time consuming procedure according to IEEE standards for ADC testing. Increasing resolutions of the produced ADCs increase contribution of analog components to the final error function. Especially, integrated sensor systems could be presented by the generalized analog to digital converter. Testing for the reduced amount of reference physical quantities from the full measuring range is much easier.

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