An FPGA System for QRS Complex Detection Based on Integer Wavelet Transform

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Abstract. *This paper presents the QRS complex detection design suitable for implementation in Field Programmable Gate Array (FPGA). It employs the simplest version of Integer Wavelet Transform for signal decomposition and techniques of zero crossing and double tresholding for extraction of R peaks which makes it suitable for application in real-time and cost effective personal healthcare assistance devices. Beside theoretical elaborations, the system architecture, simulation diagrams and working performances are presented.*

Keywords: QRS detection, FPGA, Wavelet Transform,

1. Introduction

The QRS complex is the most important segment in electrocardiogram (ECG) signal and its shape, time of occurrence and frequency gives us valuable information about heart condition. Many methods were tried on QRS complex detection, and an extensive review of the approaches proposed in the last decade can be found in [1].

The results of these studies have demonstrated that the Wavelet Transform (WT) in its discrete form - DWT (Discrete Wavelet Transform) - is the most promising method to extract characteristic points from the ECG signal. However, the most of the published algorithms are heavily processor demanding, therefore do not allow the real-time operation on personal computers.

In recent years, significant research, academic and industrial attention has been given to Telemedicine and Wearable Health Care (WHC) systems based on autonomous ultra-low-power devices capable performing real-time sampling, signal processing and wireless transfer. Such systems typically use general purpose microprocessors/microcontrollers and programmable devices.

The design of modern WHC systems therefore necessarily includes the aspects of effective algorithms, parallel processing and hardware architectures. FPGAs are kind of configurable digital circuits which can meet mentioned requirements. They mainly consist of reconfigurable logic, I/O and interconnections blocks and differ from microcontrollers and DSP processors which are Von Neumann machines. In addition to the parallelism, other advantages include: low price, flexibility of design, testing and rapid prototyping as well as ability to be transformed to Application Specific Integrated Circuits (ASICs). Also, the FPGA design can work with much higher throughput.

There are a few papers about implementing QRS detection in FPGA. Ref. [2] implements Pan-Tompkins algorithm, while Ref. [3] uses the wavelets. Both employ sophisticated filtering and other DSP blocks as well as state-machine blocks, resulting in complex design and huge occupation of silicon resources.

This paper proposes a cost and performance effective design methodology which integrates the positive characteristics of Wavelets, FPGAs and Integer Arithmetic for the purpose of QRS detection.

2. The design architecture

System Architecture

The proposed system, Fig. 1, consists of three blocks: Wavelet decomposition, Zero crossing and Double thresholding and Decision making.

Fig. 1. Architecture of proposed ECG QRS detection system

Wavelet decomposition

Unlike the Fourier transform, the DWT is suitable for application to non-stationary signals with transitory phenomena, whose frequency response varies in time, like an ECG. Mallat proposed the decomposition scheme, Fig. 2(a), which recursively employs downsampling, highpass (H) and lowpass (L) filters [4]. For each decomposition level, the H and L filters produce the details *CDi* and approximations *CAi* respectively. In order to detect the R peaks, the signal under test *x(t)* is decomposed up to a desired level, 2^1 *(CD1)*, 2^2 *(CD2)*, 2^3 *(CD3)*, 2^4 *(CD4)*, 2^5 *(CD5)*, depending upon dominant frequency components in the signal, Fig. 2(b). Then specific details *Di (i=1, 2…5)* of the signal are selected and observed.

The detection of the QRS complex is based on modulus maxima of the specific details. This is because modulus maxima and zero crossings of the WT correspond to the sharp edges in the signal. The QRS complex produces two modulus maxima with opposite signs, with a zero crossing (*ZC*) between them (Fig. 2(b), *CD4*). There are many approaches how to choose the most appropriate level for zero crossing detection. Some of them are based on the levels of signal energy through the scales.

The coefficients for the corresponding lowpass *h(n)* and highpass *l(n)* filters vary from the simplest, Haar's, over Doubisch's up to Quadratic Spline, having different vector lengths and, usually, floating point interpretation. For cost effective hardware implementation the key issue is to design as simple as possible L-H cell, maintaining all the positive characteristics of wavelets in spatial and frequency domains and satisfying the reconstruction conditions. One of the possible solutions, described in this paper, is to use one of simplest wavelet, such as Haar's, and to optimize it further for the implementation in FPGA hardware.

In our approach, the original filter coefficients are simplified in terms of integer arithmetic. The original Haar's coefficients *Lo=[1/sqrt(2), 1/sqrt(2)], Ho=[1/sqrt(2), 1/sqrt(2)]* are replaced with *L=[1/2, 1/2], H=[1, -1],* allowing the *CAj* to be calculated by an adder and shifter *CAj=(x2i+x2i+1)>>1* and the *CDj=x2i-x2i+1* by subtractor . The corresponding architecture of L-H Haar cell optimised in integer arithmetic is given in Fig. 3(a). The signal *clk_out=clk/2* is used for downsampling and storing coefficients in output registers. The decomposition scheme is reduced to the pipelined structure of L-H cells, Fig. 3(b).

Zero crosing and double thresholding

In order to detect zero crossing for chosen coefficients *CDi*, we need firstly to recognize the modulus maxima pair, Fig 4(a). Instead of using a classical way based on the local max or min, we prefer double thresholding technique. Negative and positive peaks are found by thresholding signal *x(t)* by negative and positive thresholds *TR1* and *TR2*, producing the digital signals *CRiTR1* and *CRiTR2*, with zero crossing *ZCi* between. The *TR1* and *TR2* are chosen in a range $max(x(t))/3<abs(TR1),\ TR2<max(x(t))/2$, while the *ZCi* is found by scanning the samples such that $x(n-1)<0$ and $x(n)>0$. The times t_1, t_2 and t_0 correspond to the falling and rising edges of *CRiTR1*, *CRiTR2* and *ZCi*'s trigger respectively.

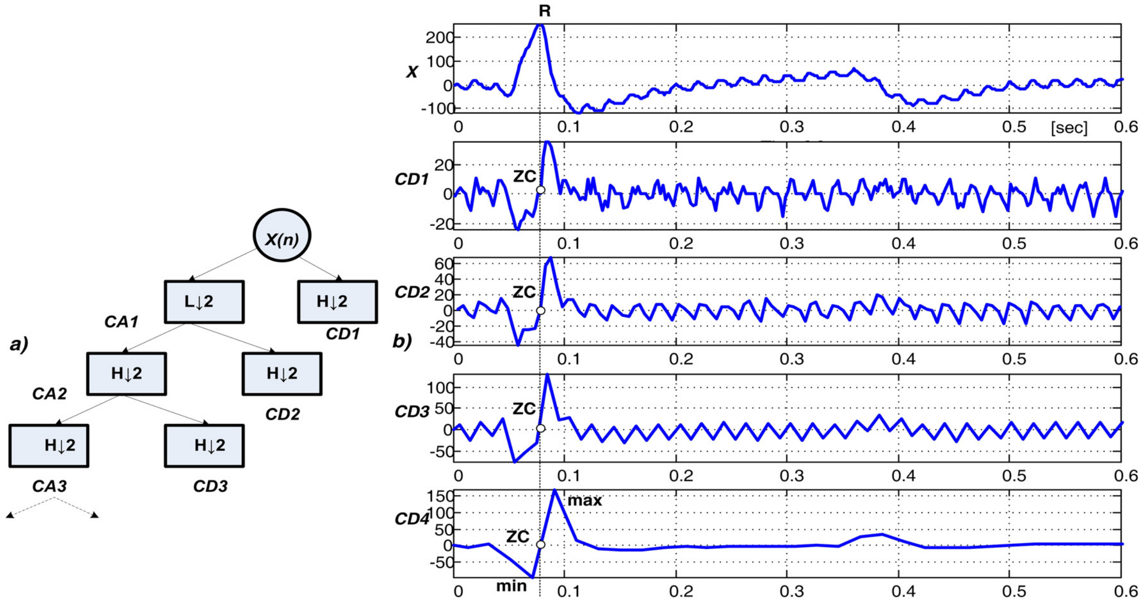

Fig. 2. a) Filter bank implementations of DWT; b) R peak detection using wavelet coefficients

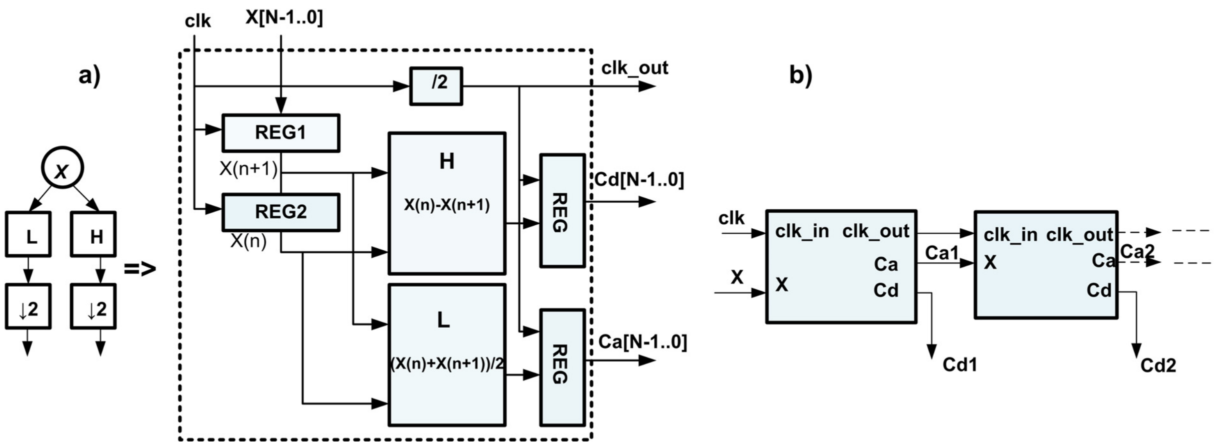

Fig. 3. a) Architecture of proposed L-H cell; b) Decomposition by pipelined structure of L-H cells

Decision making

Block for decision making receive the signals CRiTR1, CRiTR2 and ZCi for each decomposition level together with times t1(i), to(i) and t2(i). The R peak can be recognised if for each or several decomposition levels valid $t1(i)<to<t2(i)$ and $\Delta Tmin<\Delta t(i)=t2(i)-t1(i)<\Delta Tmax$, where the ΔT depends on the inclination of the QRS complex and varies from $10ms<\Delta T<50ms$ according to the ventricular activation time.

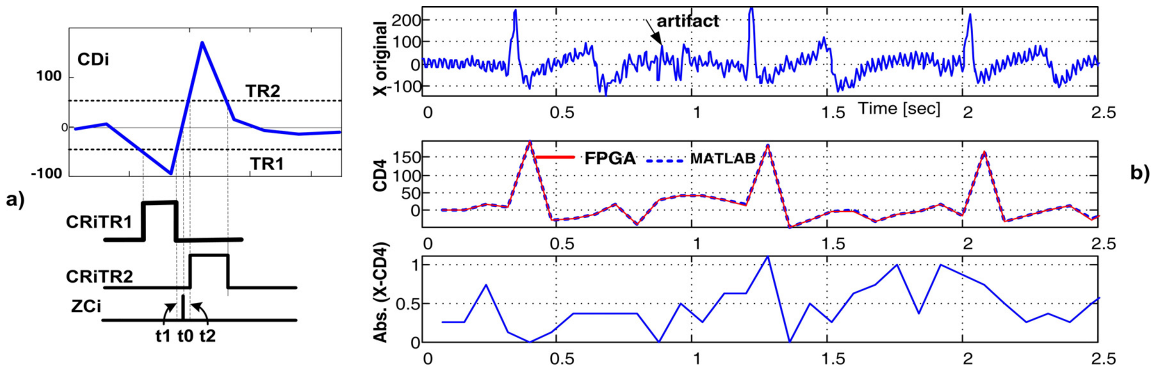

Fig. 4. a) Zero crossing and thresholding; b) FPGA-MATLAB comparison for proposed L-H decomposition

3. Results

The target FPGA chip for implementation of the proposed QRS detection system was Altera Cyclone EP1C12Q240. The data representation is with 9-bit signed integer. The performances of the system are tested in Quartus 9.1 development environment. The FPGA calculated CDi coefficients are compared with their MATLAB equivalents, Fig. 4(b). As shown, the absolute error is less than 1 count at 4^{th} coefficient. The resource consumption and maximum frequency of the whole system are listed in Table 1. After compilation and simulation the chip is configured. The signal *x(n)* presented the digital equivalents of MIT/BIH Arrhythmia database ECG and is fed to the input of system by serial port. There were totally 105,200 heart beats within *x(t)* tested. The averaged accuracy is more than 95%.

Table 1. Performances of the system

Parameter	Value
Occupation of silicon resources (LCs) for system	410 (out of 5980)
Operating frequency for system	200MHz
Averaged accuracy of QRS detection	95.23%

4. Conclusion

The paper presents a real-time FPGA-based QRS detection design suitable for autonomous embedded systems. It uses the simplest Integer Wavelet Transform for signal decomposition and techniques of zero crossing and double tresholding for extraction of R peaks.

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