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A BIST Structure for IP Multi-Slope A/D Converter Testing

R. MAGHREBI and M. MASMOUDI
GMS: Group of Micro-technology and System-on-chip
National School of Engineers of Sfax
BP W, 3038, Sfax, Tunisia
Tel: 216 74 27 40 88 Fax: 216 74 27 55 95
Correspondance e-mail: raja.maghrebi@enis.rnu.tn

Abstract—This paper proposes a static test approach suitable for built-in-self-test (BIST) of Analog-to-digital converter Intellectual Property (IP). Static parameters (INL, DNL, gain, offset) are tested without using test equipment. The proposed BIST structure is applicable for testing models of analog-to-digital converters up to 12-bits of resolution. Comparison results with dynamic test equipment validates the proposed static test approach.

Index Terms— Analog-Digital Conversion, Built-In Self-Test, Intellectual Property, Modeling.

1. INTRODUCTION

Analog and mixed signal devices need to become part of System-on-Chips (SoCs). SoCs integrate at least one processor or controller core but need to integrate real-world interfaces: filters, PLL, analog-to-digital converters and digital-to-analog converters. The key to success in developing a large scale System-on-Chips (SoCs) is to reuse analog Intellectual Property modules that have already been developed, verified and used on many previous designs. In this context, we introduce the importance to employ hardware description languages devoted for digital circuits or analog and mixed-signal circuits. To develop IP modules, the designers should begin with system-level specifications based on behavioral descriptions of the components.
Two essential subjects are treated in this paper: IP ADC module and Ramp BIST technique.
Recently, many works dealt with converter modeling and several BIST structure were proposed. In papers [1], [2] and [3], authors have employed hardware description langages to model a sigma-delta converter and a pipelined analog-to-digital converter. In [4], a linear histogram BIST scheme for A/D converter testing is optimized and implemented. In [5], the authors discuss the viability of a BIST implementation for sinusoidal histogram technique used for A/D converter testing. The BIST approach reported in [6] proposes techniques based on the linear histogram method for testing on-chip A/D and D/A converters. In [7], authors present a BIST scheme for mixed-signal circuits based on sigma-delta modulation principle.
The on-chip implementation of the histogram test technique requires a huge amount of additional circuitry. In addition, histogram test technique can mask important anomalies: for example, monotonicity or transition-level noise. Static testing is still an important method of testing A/D converters because it is a more deterministic method of testing than dynamic testing. Resultant digital output codes are compared to known analog inputs. Because of this, the transfer function of the A/D converter can be positively determined without the chance of misinterpreting the data. The implementation of this technique is feasible and do not need a huge amount of additional circuitry. The objective of this paper is to evaluate the multi-slope A/D converter model and to validate the static BIST technique.

This paper is organized as follows. Section 2 describes the analog-to-digital converter, the conversion algorithm, the static test technique and the BIST structure. Section 3 gives the multi-slope A/D converter modeling results and shows a comparison between dynamic test and static test model. Finally, section 4 gives the main conclusion of this work.

2. ADC BIST STRUCTURE

2.1. ADC DESCRIPTION

The analog-to-digital converter structure consists of three identical current-mode cells. In Fig. 1, The blocks identified as CCO, U_DC and the S/H are the main parts in each cell. They represent the current controlled oscillator, the up_down counter and the sample and hold respectively. Inputs applied to different cells are Iin, Iref and Ioff. Iin is the analog input to be converted, Ioff is the offset current and Iref is the reference current. The offset current is added in order to quantify the offset value which will be eliminated by a down-counting operation.

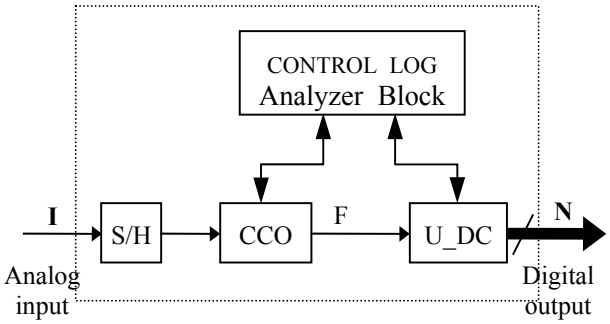

Fig. 1. Cell Block diagram

The CCO employed is a ring oscillator. It consists of an odd number of elementary cells (Fig. 2). The oscillation period depends on propagation delays t_{HL} and t_{LH}. Its expression is given in the formula (1)

$$T = n.(t_{LH} + t_{HL}) \qquad (1)$$

Where n is an odd number which represents the number of elementary cells used (three in our case). The expressions of propagation delays t_{LH} and t_{HL} obtained from hand calculations and detailed in [8], are given as

$$t_{LH} = \frac{C}{2Iref} V_{DD} \qquad (2)$$

$$t_{HL} = \alpha\, arctg\sigma + \zeta \qquad (3)$$

where:

$$\alpha = \frac{2C}{\sqrt{\beta_2\beta_4\left(V_{DD} - 2V_{Tn} - \sqrt{\frac{4Iref}{\beta_5}}\right)^2 - \left[\beta_4(V_{DD} - V_0 - |V_{TP}|)\right]^2}}$$

$$\sigma = \frac{\beta_4(V_{DD} - V_0 - |V_{TP}|)}{\sqrt{\beta_2\beta_4\left(V_{DD} - 2V_{Tn} - \sqrt{\frac{4Iref}{\beta_5}}\right)^2 - \left[\beta_4(V_{DD} - V_0 - |V_{TP}|)\right]^2}}$$

$$\xi = \frac{C\left(V_0 + |V_{Tp}| - \frac{V_{DD}}{2}\right)}{\frac{\beta_2}{2}\left[V_{DD} - 2V_{Tn} - \sqrt{\frac{4I_{ref}}{\beta_5}}\right]^2 - I_{ref}}$$

and $$V_0 = V_{DD} - |V_{TP}| - \sqrt{\frac{2.Iref}{\beta_3}}$$

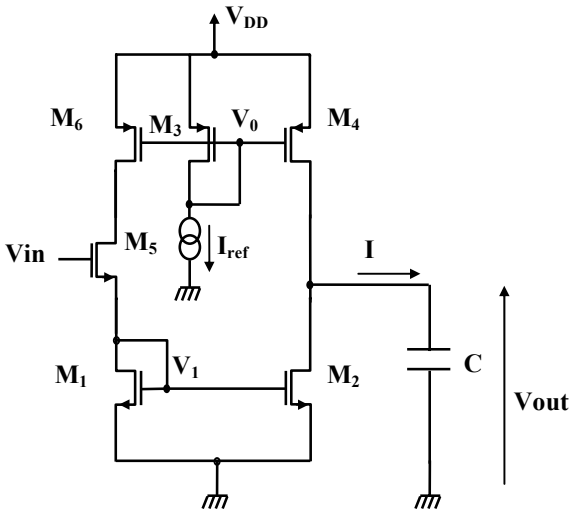

Fig. 2. Elementary cell of the CCO

Fig. 3 shows a noticeable resemblance between modeling and simulation results when comparing the curves slope and linearity. However, a variation in frequency of 10% is ascertained. These results prove the efficiency of our current controlled oscillator model.

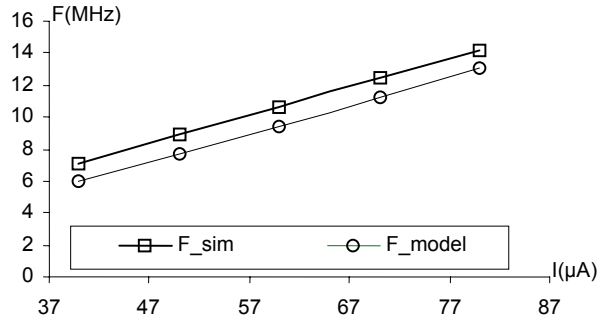

Fig. 3. Comparison between simulation and modeling results of the CCO

2.2. CONVERSION ALGORITHM

The conversion algorithm given in Fig. 4 consists in several sequences of up-counting and down-counting. A logic unit controls the end of each operation, the end of conversion and the order to convert the next sample. When the reference counter reaches the full-scale value, the two other counters' outputs have the values N_{off1} and N_{e1}.

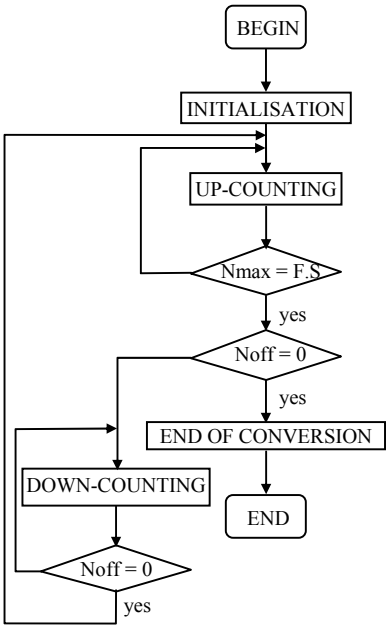

Fig. 4. Conversion Algorithm

The next operation consists in subtracting the value N_{off1} from the digital word N_{e1} by loading these outputs in the down-counters and discounting them simultaneously with the same frequency. The digital results at the down-counters outputs are N_{ref}-N_{off1}; N_{e1}-N_{off1} and 0 as. If we carry out once again the same succession, the digital outputs become N_{ref}-N_{off2}, N_{e2}-N_{off2} and 0, and so on (Fig. 5). The count-discount proceeds on until the digital output of the reference U_DC reaches its full scale value and the offset U_DC digital output becomes null. These two conditions must be filled in as a count operation is going on. The multi-slope technique eliminates the offset term N_0, offers a perfect linearity if we limit the current gap to the linear portion of the current to frequency converter characteristic. The most important achievement is the fact that the coefficient of proportionality is completely independent of technology and temperature variations as appears in the formula (4) [9].

$$N_r = \frac{N_{max}}{I_{max}} . Iin \qquad (4)$$

The conversion algorithm employed in this technique makes the circuit self-calibrated thanks to the use of three identical chains, and also to the fact that the delay time in the three cells is the same. So, state coincidence depends only on the relative value of propagation through the three chains.

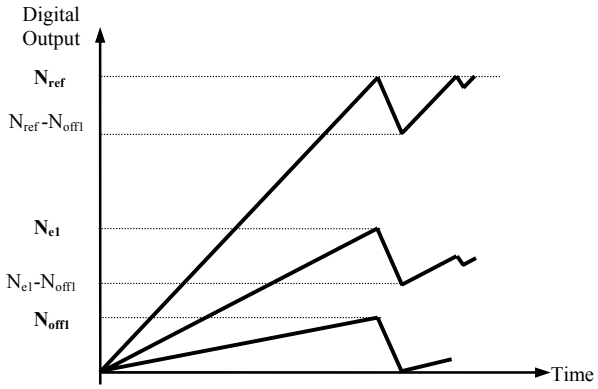

Fig. 5. Count-discount procedures of the U_DC

2.3. STATIC TEST TECHNIQUE

The ramp method is one of the most classical techniques for ADC static test [10]. A digital-to-analog converter is used to generate the input analog signal as presented in Fig. 6. Its input is incremented in very small step sizes.

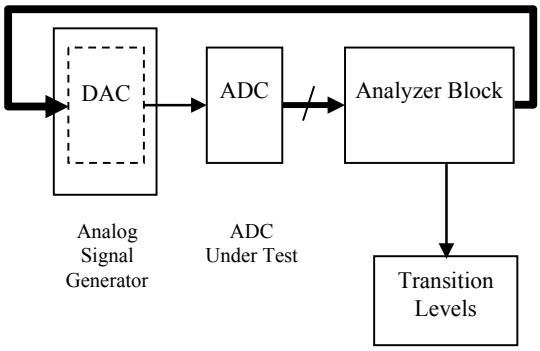

Fig. 6. Ramp Method

At each step the ADC samples the DC level a number of times. These data are collected and analyzed by the analyzer block to determine the transition level of the code. As the analog is stepped through the transition region, the conversions result in a different distribution of output codes. When the converter under test converts the new code at least 50% of the time, the analog input current is recorded as the transition level for that code. This test uses the probabilistic definition of transition levels to determine their location. The resolution of the D/A converter used in this method as an anlog signal generator should be at least 16 bits. This allows a number of samples of at least 16 if the device under test resolution is 12 bits and 32 samples if the DUT resolution is 10 bits.
After determining the location of the transition levels, specifications such as offset, gain, INL, DNL can be calculated. Also, monotonicity and amount of noise can be obtained.

2.4. BIST SCHEME

The BIST structure for analog-to-digital converters requires some resources. Fig. 7 shows the conversion block and the test block in the highest level of the hierarchy.

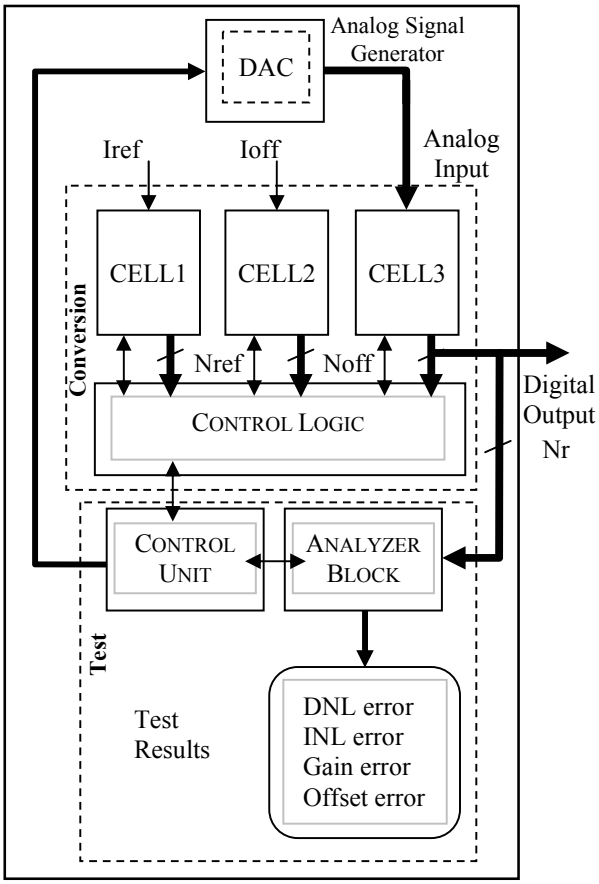

Fig.7. BIST scheme

In our case both VHDL-AMS and VHDL are used to describe different parts of the BIST structure. All digital blocks in the BIST structure are modelled using VHDL and then synthesized from VHDL. The analog blocks, mainly the current controlled oscillator is modelled using VHDL-AMS. In the conversion block, the digital-to-analog converter model acts as an analog input generator. Results obtained after the conversion cycle are treated by the analyzer block which represents the main part of the test block.

3. RESULTS AND DISCUSSION

3.1. ADC MODELING RESULTS

In a previous work, we have proved the efficiency of the current controlled oscillator (CCO) model by comparing obtained results with experimental and electrical simulation results. A good linearity has been obtained with this structure without employing techniques to improve it. Experimental results indicate that the circuit performs as expected [8]. Simulation results for the multi-slope ADC are depicted in Fig. 8 and

Fig. 9. The differential non-linearity (DNL) and the integral non-linearity (INL) obtained from the static test indicate that the multi-slope ADC model performs as expected.

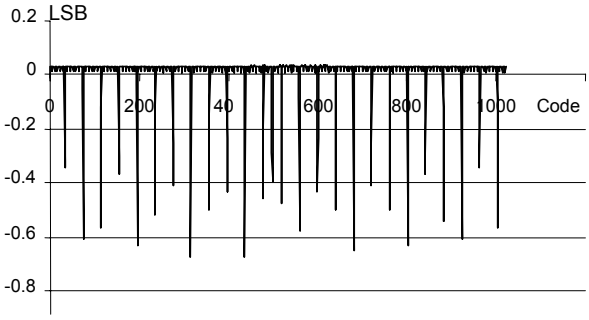

Fig.8. DNL Results from VHDL-based test

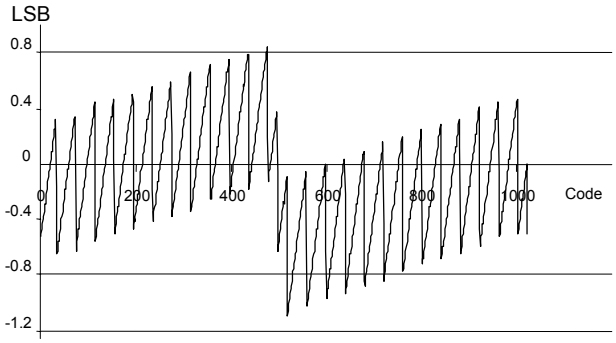

Fig.9. INL Results from VHDL-based test

3.2. TEST VALIDITY

As shown in Fig. 10 and Fig. 11, Differential Non-Linearity error and Integral Non-Linearity error results obtained from the dynamic test show a good resemblance with those obtained from the static test model. This comparison validates the ramp method modeling. The Effective Number of Bits (ENOB) given by the dynamic test is 9.27 bits for a resolution of 10 bits.

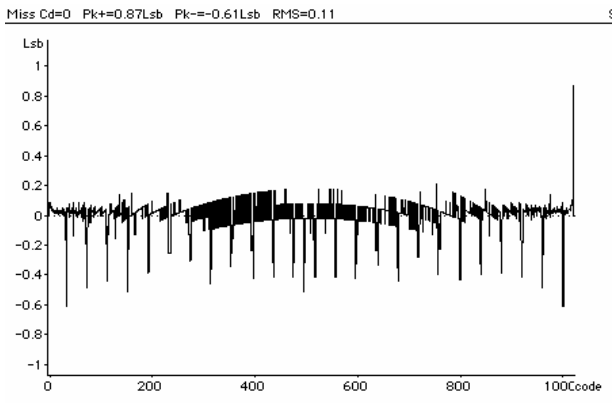

Fig. 10. DNL Results from dynamic test equipment

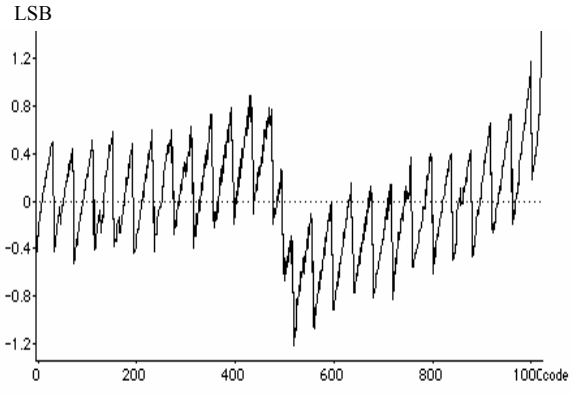

Fig. 11. INL Results from dynamic test equipment

4. CONCLUSION

This work validates the multi-slope self-calibrated A/D converter model and presents an approach for BIST structure for testing on-chip analog-to-digital converters. The BIST structure is based on the ramp technique. The main advantages of the proposed BIST scheme are the simplicity and the efficiency of the ramp technique in determining static parameters of the device under test. We show in this paper how A/D converter test results obtained from modeling (VHDL-AMS and VHDL) agree well with those obtained from dynamic test equipment. This agreement is fulfilling and shows that this IP A/D converter can be used in several applications. We will further investigate on improving the performance of BIST structure and validate our approach with hardware implementation of the ramp test technique on the same chip as the analog-to-digital converter.

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