Statistical Modeling of Bipolar Transistor Technological Parameters

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Abstract: *Thickness of base is a important technological - constructive parameter of BjT technology, which define such high temperature processes: diffusion of base, oxidation for formation of emitter windows, diffusion of emitter and oxidation for formation of contactical windows. Reciprocally these technological processes determine the thickness of base W_b. That is why are BjT technology and its special processes – diffusion and oxidation, calculation methods of base thickness too, examined. A perfect model for calculation of dash distribution in base and emitter areas is presented. It was calculated whit program MathCAD 2000 Professional. Estimating all high temperature processes is a change of base thickness shown.*

Introduction

BjT (bipolar junction transistor) technology is used for producing active radio elements and integrated semiconductor circuits. The basic of this technology is *pn* junction with specific electrical and geometrical parameters. The thickness of base is the main constructive parameter of bipolar transistors. It depends on position of *pn* junction in the plate. The quality of transistors and integrated circuits depend base thickness.

In order to measure base thickness you have to file the structure of transistor at certain language. In this case all structure is destroyed (the transistor is damaged). In case not to destroy the transistor, base thickness could be calculated knowing the depth of layer penetration. This could be done using mathematical modeling and knowing technological parameters.

Multifold high temperature processes are used in BjT technology. They go one after other and usually later processes determine previous. It is very important to evaluate this because on this depends quality of produced product.

Diffusion technology

Diffusion is the most widely used for *pn* junction production in BjT technology.

Diffusion process consists from two stages: the insertion of needed amount of impurities and dispersion of inserted impurities.

Here could be two cases of distribution of impurities atoms (laws): 1) diffusion process from finite source of impurities happens when all impurities are in very thin surface layer, 2) diffusion process from infinite source with constant diffusion concentration of surface impurities.

While calculating diffusive structures two types of problems are solved: 1) determination of profile of impurities concentration distribution, when technological process is given (direct problem); 2) determination of regimes of diffusion processes depending on parameters of impurities distribution in the structure (reverse problem).

1. Direct problems

a) Calculation of impurities distribution when two phase diffusion is given. The surface density of inserted impurity atoms is [1,2]:

$$N=\int_0^\infty N(x)dx=\int_0^\infty N_{01}erfc\frac{x}{2\sqrt{D_1t_1}}dx=2N_{01}\sqrt{\frac{D_1t_1}{\pi}}\,; \quad (1)$$

where *N(x,t)* – concentration of impurities in depth x, measured in cm, at time moment t, is measured s; N_{01} – initial amount of impurities in the source or initial surface impurities concentration, cm^{-2}; D – Coefficient of impurity diffusion, cm^2/s; erfc –additional function of uncertainties, it is equal

$$erfcy=1-\frac{2}{\sqrt{\pi}}\int e^{-\alpha^2}d\alpha\,.$$

Diffusion coefficient D is equal to number of impurity atoms, diffusing through $1cm^2$ area

per 1s, when concentration gradient of diffusing impurity atoms is 1 cm^{-4}. Dependence of diffusion coefficient on temperature could be written as follows:

$$D = D_o e^{-\frac{E_a}{kT}} ; \quad (2)$$

where D_o - coefficient depending on type of semiconductor and diffusing impurity. It is measured in cm^2/s; E_a – energy of diffusion process activation, measured eV, k - Bolcman constant, which is equal to $8{,}63 \cdot 10^{-5}$ eV/K; T – absolute temperature, K.

Distribution of reallocated impurities:

$$N(x,t) = \frac{2N_0}{\pi}\sqrt{\frac{D_1 t_1}{D_2 t_2}} \exp(-\frac{x^2}{4D_2 t_2}) = \frac{N}{\sqrt{\pi D_2 t_2}} \exp(-\frac{x^2}{4D_2 t_2}); \quad (3)$$

b) Calculation of impurity distribution when diffusion goes from finite source. Distribution of impurities:

$$N(x,t_1,t_2) = \frac{2N_{01}}{\pi} \int_{\sqrt{z}}^{\infty} \exp(-y^2) erf(\alpha y) dy ; \quad (4)$$

where y – integration constant;

$$z = \frac{x^2}{4(D_1 t_1 + D_2 t_2} ; \quad \alpha = \sqrt{D_1 t_1 / D_2 t_2} .$$

c) Calculation of impurities distribution when double diffusion is given. Total concentration distribution:

$$N(x,t) = N_{0a} \exp(-\frac{x^2}{4D_a t_a}) - N_{0d} erfc \frac{x}{2\sqrt{D_d t_d}} - N_B ; \quad (5)$$

where N_B – concentration of donors in initial plate.

2. Reverse problems

a) Determination of diffusion regimes according given impurities distribution parameters:

$$Dt = \frac{x_j^2}{4\ln(N_0 / N_B)} . \quad (6)$$

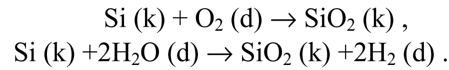
b) Determination of double diffusion regimes:

$$D_d t_d = \frac{x_{je}^2}{4[\sqrt{\ln(N_{0d}/N_{0a}) + x_{je}^2/4D_a t_a} - 0{,}3]^2} . \quad (7)$$

Coating semiconductor's surface with dielectric

Silicon dioxide (SiO_2) has two functions in semiconductors integrated circuits: 1) dielectric layer designed for insulation; 2) protective layer used for making local diffusion.

Thermal oxidation usually is made in the dry oxygen or water steam atmosphere [1,3]:



$$Si\ (k) + O_2\ (d) \rightarrow SiO_2\ (k) ,$$
$$Si\ (k) + 2H_2O\ (d) \rightarrow SiO_2\ (k) + 2H_2\ (d) .$$

Combination of these two methods is possible.

Process in the first stage could be written using linear equation $D_{oksid} / k_s = t$. In this stage the velocity of film growth is constant and is affected by velocity of surface reaction [1, 3]:

$$\frac{dD_{oksid}}{dt} = k_s ; \quad (8)$$

where k_s - constant, describing velocity of chemical reaction of Si on the surfaces, μm/s.

In the second stage the oxidation process is limited by velocity of oxidation diffusion through formed oxide. Due to this the law changes to linear – parabolic:

$$\frac{D_{oksid}^2}{k_d} + \frac{D_{oksid}}{k_s} = t ; \quad (9)$$

where k_d – constant, describing velocity of oxidation diffusion through oxide, $\mu m/s^2$.

In this stage decrease of SiO_2 growing rate could be written as follows:

$$\frac{dD_{oksid}}{dt} = \frac{k_d k_s}{2D_{oksid} k_s + k_d} . \quad (10)$$

In the third stage the growth of SiO_2 film is limited by oxidation diffusion through oxide film. Process is written in parabolic form:

$$\frac{D_{oksid}^2}{k_d} = t\ . \qquad (11)$$

In the third stage the growing rate apace decrease when thickness of SiO_2 plate increases. It could be found from following equation:

$$\frac{dD_{oksid}}{dt} = \frac{k_d}{2D_{oksid}}\ . \qquad (12)$$

In the fourth stage the thickness of SiO_2 film approaches the $D_{oksid.max}$ value which depends on oxide type, its pressure, process temperature. Oxidation in this stage almost has no influence. Due to this oxidation is cancelled at the end of third stage.

Coefficients k_d and k_s are dependent on the temperature, the SiO_2 film thicknesses and times of production are also dependant on temperature. In order to get thicker film, it is more economic expedient to finish process at the end of third stage – at the beginning of the fourth.

Thermal oxidation is technological process. Obtained SiO_2 film is of high quality, but due to high process temperature, changes of dimensions in formed pn junctions, redistribution of impurities are happening.

Calculation of BjT technological regime

The distribution of impurities concentration in *npn* junction obtained in double diffusion way are calculated. Diffusion regimes are taken from statistical data: T_a = 1200 º C, t_a = 1 h, T_d = 1100 º C, t_d = 2 h. The surface concentration of boron is $N_a = 5*10^{14}$ cm^{-2}, phosphorus diffusion is going from infinite source. Oxidation is going in wet oxygen for 1 h. the impurity concentration in the initial plate is $N_B = 5*10^{16}$ cm^{-3}. Diffusion coefficients are: $D_a = 2*10^{-12}$ cm^2/s, $D_a^* = 2.5*10^{-13}$ cm^2/s, $D_d = 1*10^{-13}$ cm^2/s. Also $N_{0d} = 1,2*10^{21}$ cm^{-3}.

Impurities distribution is calculated according formula (5). But this formula does not evaluate oxidation which goes after. That's why it has to be written as follows:

$$N(x,t) = N'_{0a}\exp(-\frac{x^2}{4(D_a t_a + D_a t_{oks} + D_a t_d + D_a t_{oks})} - \\ - N_{0d}\,erfc\frac{x}{2\sqrt{(D_d t_d + D_d t_{oks})}} - N_B; \qquad (13)$$

where

$$N'_{0a} = \frac{N_a}{\sqrt{\pi(D_a t_a + D_a t_{oks} + D_a t_d + D_a t_{oks})}};$$

t_{oks} – oxidation time.

Calculation were made using MathCAD 2000 Professional program. Calculation results are shown in fig. 1.

Evaluating high temperature processes going after diffusion ones, obtained impurities redistribution is shown with thick continuous lines. This matches real situation of BjT technology.

Also are shown base thicknesses – initial W_p and final W_g , obtained after estimation of all high temperature processes.

Conclusions

1. After analyzing BjT technology was determined that most important integrated transistors and integrated circuits parameter is base thickness. This parameter depends on high temperature technological processes – epitaxy, oxidation and diffusion regimes.

2. It was determined that base thickness could be measured not only by destroying structure but also calculating knowing impurities distribution in diffusive layers.

3. It was taken existing impurities distribution calculation model. After investigations it was found that it does not evaluate all high temperature processes. That is why was created improved model which is able to evaluate this.

4. Calculations were made according both models. While calculating impurities distribution according first model, taken initial data matched the real production situation. From obtained results could be seen that base thickness is about 0,6 μm. It has to be like this. In another case if it will be bigger than 1 μm, the device working speed will be decreased. It should not be decreased as well. In this case rupture occurs.

5. After calculation according second method with the same initial conditions, we could see from the results that base thickness increased more than 5 times. This has happened because formation of base region is followed by few high temperature processes. At high temperature impurities in the formed base region diffuses deeper.

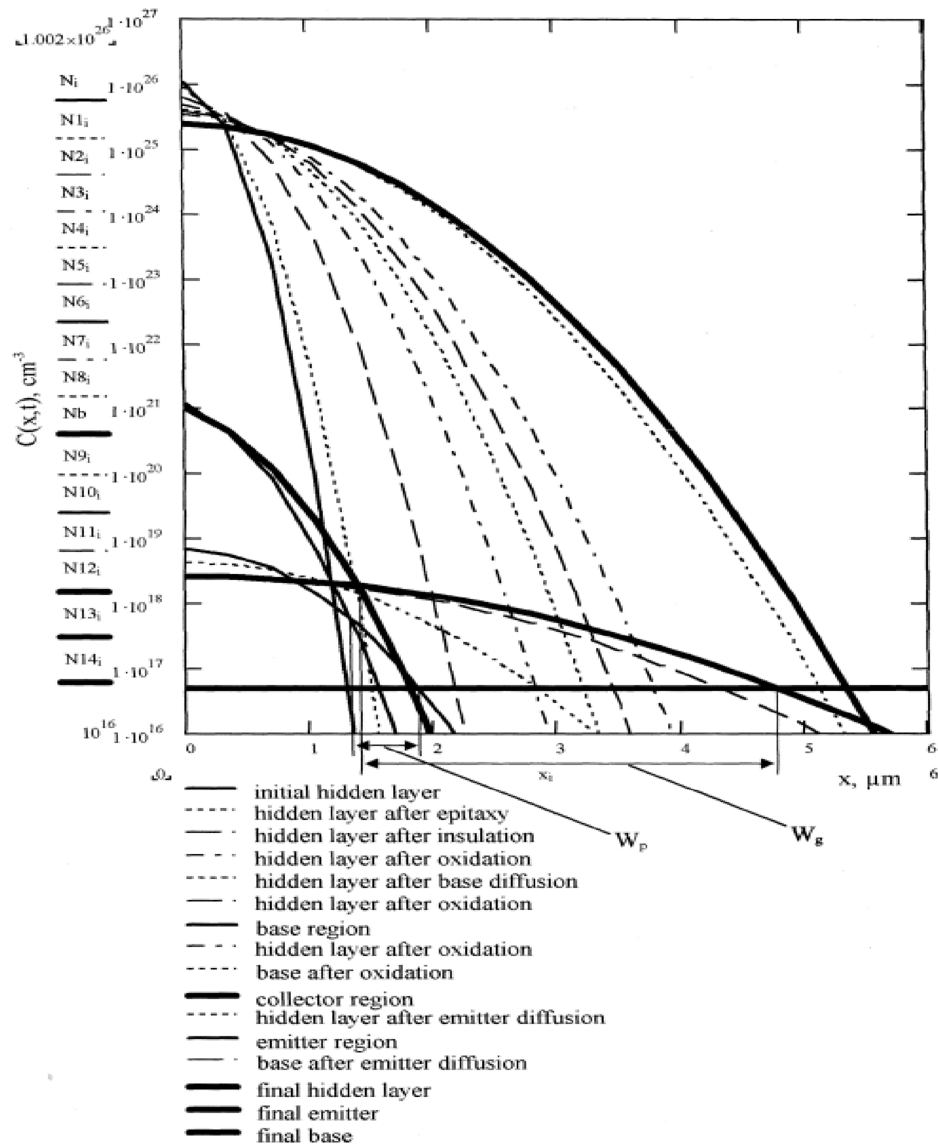


Fig. 1. Distribution of impurities in *npn* junction

6. After investigation of BjT technology and evaluating possibilities of improved method, some decisions, which would secure integrated transistors parameters, could be done. Decisions are as follows:

a) Decrease time of technological processes which have influence to base region,

b) During base and emitter diffusion only impurities insertion should be done. Disengagement will be done by following high temperature processes,

c) Decrease impurities diffusion coefficients while decreasing process temperatures.

Literature

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