Measurement of generation parameters on $Ru/HfO_2/Si$ MOS capacitor

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Abstract. *We report extended analysis for measurement of generation lifetime and surface generation velocity, s_g, on advanced gate stack with high-κ dielectric using leakage current characteristics in inversion condition. Proposed technique was examined on $Ru/HfO_2/Si$ MOS capacitor annealed in forming gas (90% N_2 + 10% H_2) at temperatures 430 and 510 °C. It was found that s_g decreases with FGA temperature increasing, however, density of interface traps, D_{it}, unexpectedly increases after second FGA. The results are discussed together with capacitance vs. gate voltage measurement.*

1. Introduction

As the thickness of SiO_2 film used in complementary metal-oxide-semiconductor (CMOS) technology reaches the sub-1.0 nm, significant leakage current (above 1 A/cm^2) due to direct tunneling and reliability become major issue. Therefore, thicker dielectric with higher dielectric constant (high-κ) should replaced conventional SiO_2 which results in maintaining of capacitance per unit area and decreasing of leakage current trough the oxide. Up to date, HfO_2 is widely accepted as the potential dielectric for SiO_2 replacement [1]. Another scaling issue arises from polycrystalline Si used as the gate electrode, since it reveals depletion effect. Moreover, boron penetration after its implantation into poly-Si in pMOS transistors markedly reduces the channel mobility [2]. It is obvious that utilizing of metal gate into new CMOS technology can suppress these effects. Furthermore, usage of dual metal gates with work function, Φ_m, of 5.2 and 4.1 eV for pMOS and nMOS transistors, respectively, facilitates tuning of transistor's threshold voltage [3]. It is still unclear which metals neither the deposition technique can fulfill the process integration issues. Recently, we have showed that ruthenium grown by metal-organics chemical vapour deposition (MOCVD) is suitable material for gate electrode of a pMOS transistor [4].

It is well known that quality of oxide-Si as well as near-surface Si bulk has a crucial influence to the device performance. Despite the intensive research into high-κ gate oxides, mentioned regions are of weak quality resulting in low carrier mobility. Hence, further optimization of deposition conditions and subsequent annealing is needed. Measurement of generation parameters, *i.e.* surface generation velocity, s_g, and generation lifetime, τ_g, represents excellent tool for such purpose, since these entities are directly related to electrical activity of defects at the oxide-Si interface and in the subsurface Si bulk, respectively. The generation parameters are routinely determined from capacitance transient (*C-t*) response of MOS capacitor during its revert from deep-depletion into equilibrium strong inversion state. However, MOS capacitors with high-κ dielectrics are usually rather leaky making *C-t* measurement impracticable. Nevertheless, Liu *et.al.* [5] has shown that τ_g can be evaluated from the leakage current of MOS capacitor measured in strong inversion region. In this paper, we have extended this analysis for determination of s_g on advanced MOS capacitor.

2. Theoretical background

We will consider a MOS capacitor composed of p-type substrate, thin high-κ oxide and metal gate. In the case that negative bias is connected to the electrode, metal represents the cathode and electrons are injected from the metal into the oxide. The leakage current is then controlled by tunneling or Schottky emission process trough the oxide. Under positive bias condition, silicon substrate has to supply electrons for current flow. It was shown that leakage current is limited by supplying of electrons in the silicon while tunneling or Schottky emission to the corresponding band in dielectric neither electron drift in the dielectric are not limiting factors [5]. Since Si substrate is not able to provide for sufficient amount of minorities, capacitor is driven into deep-depletion state with positive gate voltage increasing. In this state, generation process is responsible for supplying the electrons and generation current density is given as [7]

$$J_{gen} = \frac{qn_i W_g}{\tau_{geff}} + qn_i s_{geff} , \tag{1}$$

where τ_{geff} is effective generation lifetime, which consists of bulk space charge region (scr) and surface scr generation, s_{geff} is effective surface generation velocity composed of surface generation under the gate and diffusion from quasi-neutral bulk, q is the charge of an electron, n_i is the intrinsic concentration and W_g is the generation width. We consider generation width to be given by scr width, W, subtracted by its width under equilibrium inversion state, W_{inv}, thus, $W_g = W - W_{inv}$. Moreover, we assume surface potential, φ_s, in inversion condition equal to gate bias voltage, V_g, due to high capacitance of the gate dielectric (high-κ). Then, we have $\varphi_s \cong V_g \propto 1/C^2$ and generation lifetime can be obtained from $J_{leak} \equiv J_{gen}$ *vs.* $\sqrt{V_g}$ plot. This was done by Lui *et.al.* in Ref. [5].

From the egn. 1, it is clear that s_{geff} can be extrapolated as the intercept of J_{gen} vs. W_g plot. If the dielectric is sufficiently thin, the electrons will be injected into the dielectric immediately after inversion layer creation. On the basis of this assumption and generation width mentioned above, the J_{gen} can be expressed as

$$J_{gen} = \frac{qn_i}{\tau_{geff}} \sqrt{\frac{2\varepsilon_0 \kappa_{Si}}{qN_A}} \left(\sqrt{V_g} - \sqrt{2\varphi_F + V_{FB}} \right) + qn_i s_{geff} , \tag{2}$$

where N_A is the doping density, ε_0 is the permittivity of the vacuum, κ_{Si} is the permittivity of Si, V_{FB} is the flat-band voltage shift, φ_F ($= kT \ln[N_A/n_i]$, k is the Boltsmann's constant and T is absolute temperature) is the Fermi potential and W_{inv} was expressed as

$$W_{inv} = \sqrt{\frac{2\varepsilon_0 \kappa_{Si} (2\varphi_F + V_{FB})}{qN_A}} . \tag{3}$$

Then τ_{geff} as well as s_{geff} can be evaluated as the slope and intercept of J_{gen} vs. $\left(\sqrt{V_g} - \sqrt{2\varphi_F + V_{FB}} \right)$ plot, respectively.

3. Experimental and results

In order to examine proposed extended analysis, we have prepared advanced Ru/HfO_2/Si capacitors. The Ru films were grown using Aixtron TriJet^{TM} liquid precursor technology in a low-pressure hot-wall quartz MOCVD reactor at 350 °C. As substrates we have used p-doped Si with HfO_2 prepared by atomic-layer chemical vapour deposition with dielectric thicknesses ranges from 2 to 6 nm. The structure was then subjected to a forming gas annealing (FGA, 90% N_2 + 10% H_2) at temperatures 430 and 510 °C. Capacitance vs. gate voltage (*C-V*) and leakage current characteristics (*I-V*) were measured using Agilent 4248A LCR-meter and a Keithley 6517A Electrometer, respectively.

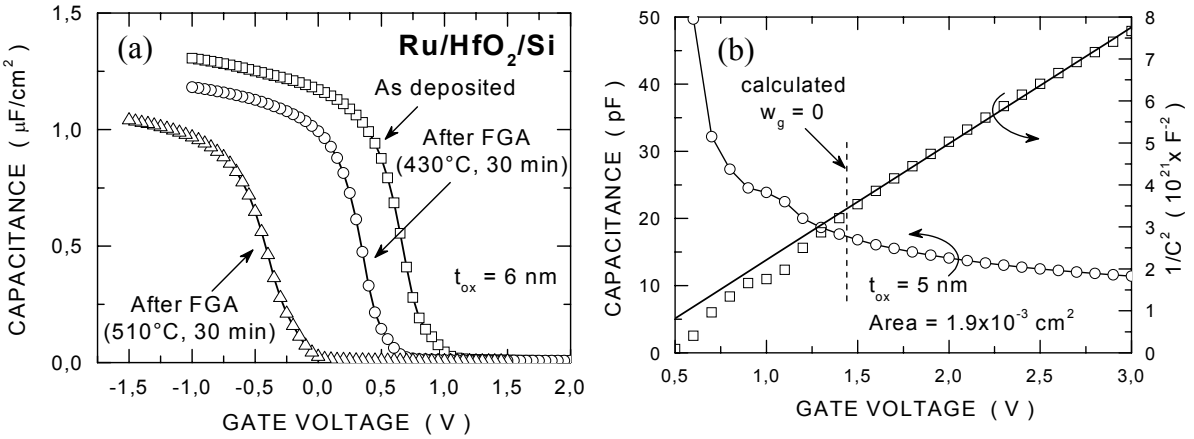

Fig. 1 (a) *C-V* curves of as deposited and forming gas annealed Ru/HfO_2/Si MOS capacitors (f_{meas}=100 kHz). (b) *C-V* and $1/C^2$ plot of as deposited sample.

Fig. 1(a) shows *C-V* curves of as deposited and FG annealed Ru/HfO_2/Si MOS capacitor. The V_{FB} shift was caused by both, metal work function as well as N_{ox} change (Tab. 1) which was extracted from V_{FB} vs. equivalent oxide thickness plot [7]. From these curves, V_{FB} was extracted in order to determine the beginning of strong inversion condition, thus voltage at which W_g=0. This is illustrate in Fig. 1(b) where C and $1/C^2$ as the function of gate voltage is plotted together with calculated V_g for W_g=0. It can be seen that beginning of deep-depletion state due to lack of minorities and calculated voltage for zero generation width correlate well.

I-V characteristics of as deposited MOS capacitors as well as samples annealed in FG at 510 °C (inset) are depicted in Fig. 2(a). Using these curves, doping density for φ_F calculation and V_{FB}, we have constructed the J_{gen} vs. $\left(\sqrt{V_g} - \sqrt{2\varphi_F + V_{FB}}\right)$ plots for MOS capacitor with dielectric thickness t_{ox}=5 nm and extracted generation parameters are summarized in Tab. 1. D_{it} was determined using simple conductance method [8]. Since maximum of the plot G_m/ω vs. log$f$ was observed at 100 kHz, this frequency was chose for D_{it} calculation.

4. Discussion

FGA is routinely used in CMOS process for passivation of oxide-Si traps, hence it can be expected that such treatment will influence mainly s_{geff}. Recently, we have shown by means of D_{it} that higher FGA temperature for Ru/HfO_2/Si gate stack is needed for passivation of oxide-Si interface traps [7]. Similar behavior can be observed also for generation parameters. Absolute value of J_{leak} at the beginning of generation process corresponds to s_{geff} while curvature corresponds to τ_{geff}. It is mainly s_{geff} that reveals big dispersion for as deposited capacitors whereas one can see almost the same currents after FGA at 510 °C for MOS capacitors with different dielectric thickness.

Values of τ_{geff} and s_{geff} were measured on MOS capacitor with t_{ox}=5 nm (Tab. 1). After FGA at 430 °C, only slight improvement was observed. Nevertheless, τ_{geff} is more than two times higher and s_{geff} decreases abruptly after FGA performed at 510 °C. However, we observed increasing of D_{it} which is in contradiction to s_{geff} tendency. We note that these entities are connected via formula $s_g = \sigma_{it} v_{th} D_{it}$, where σ_{it} is the interface capture cross-section and v_{th} is the thermal velocity (for Si v_{th} =1×10^5 ms^{-1}). This behavior can be explained by further growing of SiO_2 interfacial layer, since oxide capacitance has decreased after FGA at temperature 510 °C (see Fig. 1(a)). Also N_{ox} change in sign which support this assumption because it is known that SiO_2 reveals positive oxide charge. Consequently, there are two

Tab. 1 Summary of experimental data.

Thermal treatment	τ_{geff} (μs)	s_{geff} (cm/s)	N_{ox} (cm^{-2})	D_{it} (eV^{-1}cm^{-2})
As deposited	6	5.8	-5.8×10^{12}	4.5×10^{11}
FGA (420 °C, 30 min)	6.8	4.1	-2.4×10^{12}	2.3×10^{11}
FGA (510 °C, 30 min)	15	0.9	5.3×10^{12}	5×10^{11}

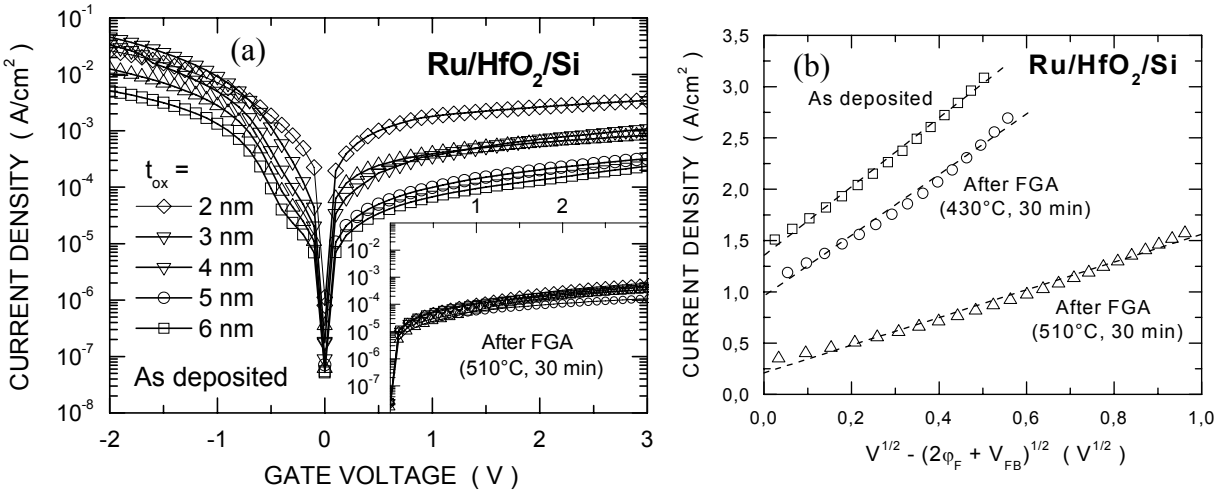

Fig. 2 (a) *I-V* characteristics of as deposited and FG annealed (inset) MOS capacitor at 510 °C for different dielectric thickness. (b) Extraction of τ_{geff} and s_{geff}.

interfaces, Si-SiO_2 and SiO_2-HfO_2, which can exchange the charge during ac measurement. However, s_{geff} was measured at dc signal which can cause big discrepancy in capture cross-section, hence discrepancy between D_{it} and s_{geff}.

5. Conclusion

We have presented simple technique for evaluation of effective surface generation velocity from *I-V* characteristics under inversion conditions bias for MOS capacitors with thin high-κ gate dielectrics. Proposed procedure was examined on Ru/HfO_2/Si MOS capacitors annealed in FG at temperatures 430 and 510 °C for 30 min. As it was expected, s_{geff} decreases with FGA temperature increasing, however, D_{it} increased under its as deposited value. This discrepancy can be explained by interface capture cross-section increasing due to charge exchange between Si-SiO_2 and SiO_2-high-κ interfaces. We conclude that proposed simple technique can improve the optimization process of new CMOS technology.

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