

“Follow Me” - Digital Jitter Measurement Method

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***Abstract.** This paper consists description of research results regarding digital jitter measurements for higher data rates. In previous publications [1][2][3] author has investigated different methods of digital jitter measurements, however they were applicable for data streams with lower clock frequencies. Developed methods and algorithms were optimised for implementation in FPGAs or ASICs. This work consists description of novel digital jitter measurement technique using programmable clock generators with phase shifters. Tests of this method were performed on well-known FPGA chips however may be easily extended to other digital environments. Obtained results are very promising; whole system may be integrated in one chip, measurement accuracy and resolution is pretty good and solution is easily scalable.*

Keywords: Jitter, Phase Noise, SDH

Introduction

Jitter is a time domain name of a phenomenon called phase noise in a frequency domain. Origins of phase noise are: different sources related to the conductors nature (thermal noise, shot noise, 1/f noise, g-r noise, etc.), power supply noise and spikes, channel and symbol interference, etc. Fact the ideal pure harmonics do not exist manifests in disparity between time events in the time domain. This process is based on different statistics, most of them have Gauss nature.

Jitter is a serious problem for communication system engineers. Modern telecommunication networks translate this phenomenon to the serious problem on different levels – beginning with a physics layer and ending with a protocol layer. Therefore designers try do minimise this phenomenon. However, to be effective they need to perform tests on networks and devices against jitter. In spite of the stochastic nature, the best testing methods use deterministic signals, like clock wave modulated with single sine wave.

Methodology of tests is well known and documented by ITU-T [3] and other authorities. Also in the market there are many analog devices or mixed digital and analog solutions for this purpose. However it is very challenging but very promising also to design test solution based on digital technique only integrated within one chip for different data rates. Digital nature of this solution will guarantee:

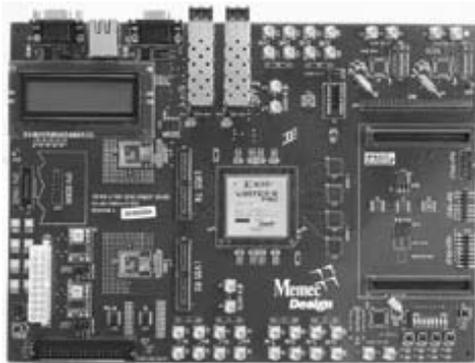
- thermal and time stability,
- measurement repeatability,
- a wider span between calibration procedures,
- reduction of maintenance and service cost.

This paper consists description of such solution, which may replace old fashioned methods based on sampling techniques not scalable to higher data rates. Strong advantage of this idea is the same core may be used for a jitter generator and meter.

Jitter Analysis Methods

Analog methods as well known would not be discussed here. It is possible to find many references about them; also as stated in previous section this category of methods does not lay in focus of our attention due to poor parameters.

In an author opinion on digital systems there are three main methods of jitter measurement: a sample and count method [1][2], an interlaced sample and count method and novel “follow me” method. Regarding jitter generation there are two methods: digital modulation technique and novel “follow me” method.



Test platform used in experiments.

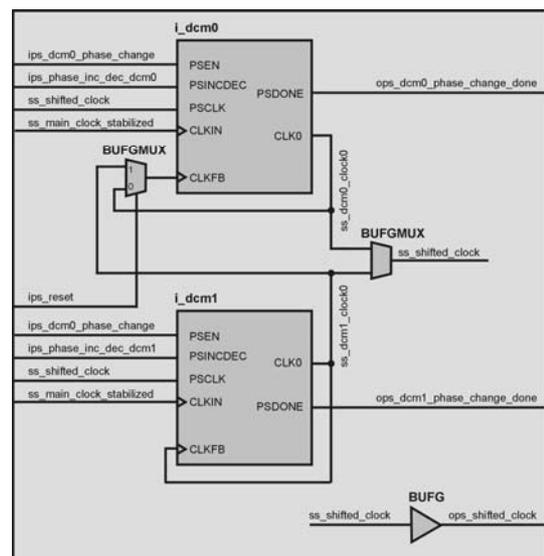
The sample and count method bases on a modified phase comparator. This module not only compares phase difference but also counts quantity of whole clock periods measured clock signals differ. This is in opposition to standard procedure comparing phase modulo clock cycle period. For this method serious problem lays in sampling frequency, i.e. measure accuracy depends on it (e.g. accuracy 0.01 part of clock cycle means sampling frequency 100 times higher than clock frequency) [2]. The interlaced sample and count method is an extended version of previous. Samples of a clock signal are taken with some interval depends on needed accuracy and

measured jitter frequency. This method allows theoretically investigating higher data streams but has only theoretical meaning and is not acceptable for commercial applications, due to statistical phase noise nature. Generation of jitter with digital modulators was discussed in many papers [1][2]. Therefore it is only important to say, that sampling theorem is again serious problem.

“Follow me” method is a breakthrough without disadvantages of previous systems, especially with sampling limits. Its parameters depend only on digital implementation, what will be discussed in a next section.

The “Follow Me” Method

Follow me method bases on observation phase changes of clock signal in telecommunication systems are relatively slow, therefore fast sampling may be replaced with accurate tracking of slow clock edge movements. This may be performed with accurate digital phase shifters and special algorithm of driving them. These algorithms have to follow phase changes with programmable phase shifters to minimise disparity between a measured signal and generated. Steps of a phase shifter are simultaneously results of jitter measure. Also the same core may be used in the jitter generator – in this case digital phase shifters have to reach a given phase shift.



Phase shifter structure.

Implementation

The mentioned circuit was implemented within Virtex II Pro chip form Xilinx mounted on evaluation board from Memec (Fig. 1). This platform offers digital transmitters for SDH data streams as well as programmed Digital Clock Managers (DCM) [5]. The author has implemented the digital jitter meter and generator within mentioned chip for a STM-1 data stream.

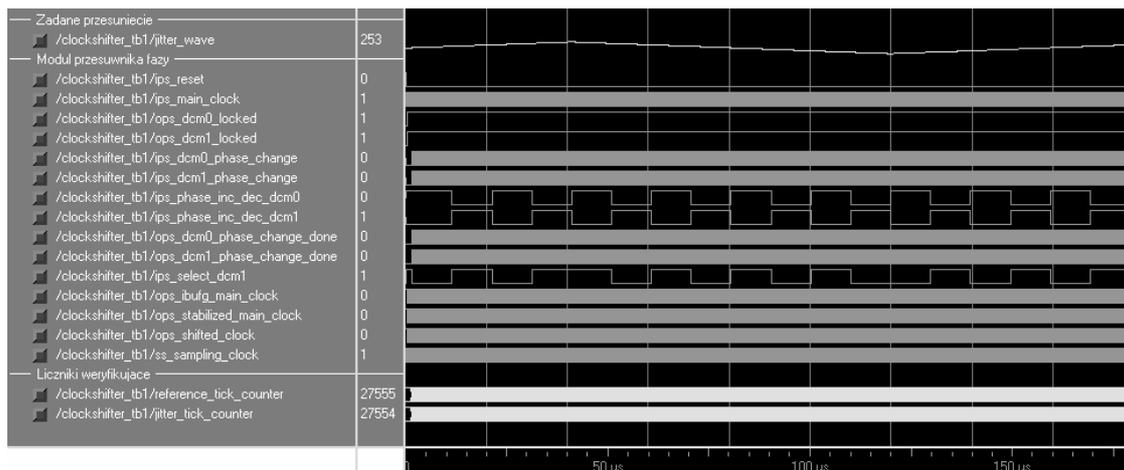
Structure of a Phase Shifter

Whether we talk about the “follow me” generator or meter, the main part of both modules was phase shifter built with DCMs. The structure of phase shifter is depicted on Fig. 2. Specialised state machines drive signals with algorithm, which controls disparity between obtained and required phase shift.

Results

Simulation

Fig. 3 depicts results of low-level simulation of the built clock phase shifter. Wave called “jitter_wave” relates to the requested phase shift value. Output from phase shifter is wave “ops_shifted_clock”.



Results of phase shifter simulations

Accuracy

Proposed “Follow Me” jitter analyser for STM-1 stream has accuracy required by the ITU-T 0.172 [4] document and meets all requirements in check points – see Table 1. Presented results come from calculations and tests.

In the case of Virtex II Pro and STM – 1 accuracy of the analyser is 0.015 UI (where UI is one clock cycle – Unit Interval [1]) and depends on intrinsic circuit jitter equals to 100ns (for the 6.43ns clock period). Accuracy of discrete phase shifter (30ps) is not so important and results in resolution equals to 0.005UI for STM-1.

Conclusions

Presented solution is very promising due to digital nature, fact it can be implemented in one chip and its good accuracy (0.015UI) and resolution (0.005UI). It may be easily scalable and reused for higher data streams (but also lower). Also, the “follow me” analyzer may concur

with professional jitter meters available on the telecommunication market (meets ITU-T requirements and is easy to implement). Table 2 consists comparison the “follow me” solution with another solutions. It may be easily observed the “follow me” method is better than others.

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ITU-T O.172 check points.

Frequency	Required amplitude	“Follow me” amplitude
125 mHz	50 UI	110 450 UI
19.5Hz	50 UI	708 UI
500Hz	2 UI	27.61 UI
6.5kHz	2 UI	2.12 UI
65kHz	0.2 UI	0.21 UI

Comparison the “follow me” solution with another solutions.

Parameter	Method	Analog	Digital (sampling)	Digital “Follow Me”
An upper baud rate limit		Limited only by analog PLL	PDH data rates	Limited only by digital phase shifters
The range of generated and measured jitter parameters		Low - limited by PLL parameters	Wide – limited by the sampling theorem	Wide – limited by the shifting period
Long time stability		Low	High	High
Immunity to the external conditions		Low	High	High
Calibration		Often	Seldom	Seldom
A place in telecom system		Only PLL	Depends on application	Depends on application
Level of complication		Low	High	High
Cost		Low	Medium	Low
Furtherer data processing		Poor	Great	Great

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