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Integral Nonlinearity Correction Algorithm Based on Error Table Optimizing and Noise Filtering

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The main purpose of this paper is to present the external correction of analog to digital converters (ADC) integral nonlinearity and quantization noise based on the look up table method (LUT) combined with the averaging and Wiener filtering and dithering method. The LUT compression and LUT precision effect are also studied.

Keywords: integral nonlinearity, look up table method, averaging filter, dithering, memory requirement

1. INTRODUCTION

CORRECTION of integral nonlinearity (INL) is required for the commonly used ADCs working out of the operational conditions for the distortion reduction. Several methods were designed to reduce nonlinearity such as Bayesian filtration, Volterra filtration or Look up table method.

2. DESIGNED CORRECTION STRUCTURE

The designed correction structure can be seen in Fig. 1. The dither signal is added to the input analogue signal with the aim to eliminate high frequency part of ${}^{HCF}INL$ [5]. The dither signal has to be uncorrelated with the input signal.

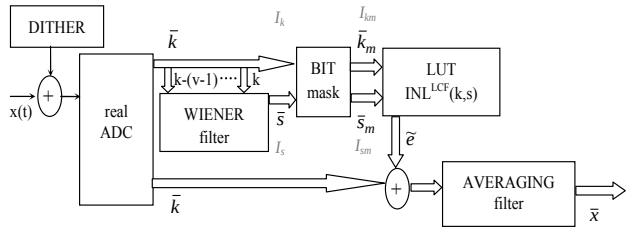

Fig.1 The designed INL correction structure based on LUT

The peak to peak value of the dithering signal larger than maximal ${}^{HCF}INL$ represents the second necessary condition. The frequency of dither signal should be set to the value f_d (see Eq. 1) to suppress the dithering signal in the non subtractive structure [4] by averaging filter.

$$f_d = \frac{frequency\ of\ input\ signal\ .\ number\ of\ samples}{2^L} \qquad (1)$$

The signal after analogue to digital conversion enters first the **Wiener filter** to estimate slope and after that it enters the **bit mask device (BMD).** The main goal of the BMD is the reduction of the error table address length. The highest bits of the slope are very rare, so they can be ignored. The new two dimensional **error table** (ET) address $(\bar{k}_m, \bar{s}_m)$ is obtained after error table compression, ignoring the lowest bits of slope $\bar{s}$ and code $\bar{k}$ from the actual sample. It means that the original address space with the size of (I_k,I_s) is reduced to the space of the size (I_{km},I_{sm}).

The content of the ET is the rounded value $\tilde{e}(k,s) = round\left\{{}^{LCF}INL(k,s)\right\}$, where ${}^{LCF}INL$ represents the low frequency code part of *INL*, obtained in the testing phase of the size $2^{I_k m + I_{sm}}$. The ET is being compressed by the substitution of the median value in the ET cell from the adjacent cells. The median is the middle value of the uplink row values. The error table elements are saved with precision β bits after decimal point. The quantization noise declines virtually according to the virtual quantization step Δ (Eq.2), where *Q* is code bin width:

$$\Delta = 2^{-\beta} Q \qquad (2)$$

The actual code *k* is corrected in two steps. The ${}^{LCF}INL$ is reduced by the added ET correction value $\tilde{e}$. The ${}^{HCF}INL$ is suppressed by the averaging filter. The final output signal is $\bar{x}$. The averaging filter of length 2^L virtually increases the ADC resolution. The output sampling frequency f_s is determined from the input oversampling frequency f_{os} and the reduced quantization noise E_{kv} is determined by Eq. 3:

$$\frac{f_{os}}{2^L} = f_s > 2 f_{\max} \quad \Rightarrow \quad E_{kv} = \frac{Q}{\sqrt{12}\sqrt{2^L}} \qquad (3)$$

Here *Q* is the code bin width of the ADC and f_{max} is the maximal input signal frequency.

3. EXPERIMENTAL RESULTS

The designed structure was studied by the computer simulation using real converter model represented by the ideal converter with superimposed low and high code frequency *INL*. The simulated representatives of the real ADCs were described by the maximal *INL* differences $\Delta INL_{max}(k=0)$ along *s* axes and $\Delta INL_{max}(s=10)$ along code *k* axes in the *INL* phase plane (first column Tab.1). The Tab. 1 shows the simulation results in the percentage ENOB improvement, which were determined by the comparison to the non corrected signal from the ADC output. The second column of Tab.1 shows the ENOB improvement based on the ET. The third column shows the ENOB improvement of the whole correction structure.

INL(s,k)	*correction efficiency with LUT considering only*	*correction efficiency with LUT, Wiener filter (order 3), averaging filter (order 5) and dithering (amplitude2LSB)*
$\{INL_1\}$ $\Delta INL_{max}(k=0) \cong 30$ LSB, $\Delta INL_{max}(s=10) \cong 11$ LSB	32.1 %	37.6 %
$\{INL_2\}$ $\Delta INL_{max}(k=0) \cong 1$ LSB, $\Delta INL_{max}(s=10) \cong 12$ LSB	34.6 %	39.1 %
$\{INL_3\}$ $\Delta INL_{max}(k=0) \cong 2$ LSB, $\Delta INL_{max}(s=10) \cong 13$ LSB	34.5 %	39.4 %
$\{INL_4\}$ $\Delta INL_{max}(k=0) \cong 8$ LSB, $\Delta INL_{max}(s=10) \cong 48$ LSB	38.6 %	43.3 %
$\{INL_5\}$ $\Delta INL_{max}(k=0) \cong 4$ LSB, $\Delta INL_{max}(s=10) \cong 48$ LSB	38.7 %	43.6 %
$\{INL_6\}$ $\Delta INL_{max}(k=0) \cong 30$ LSB, $\Delta INL_{max}(s=10) \cong 18$ LSB	24.2 %	32.9 %
$\{INL_7\}$ $\Delta INL_{max}(k=0) \cong 17$ LSB, $\Delta INL_{max}(s=10) \cong 12$ LSB	33.6 %	38.5 %
$\{INL_{11}\}$ $\Delta INL_{max}(k=0) < 1$ LSB, $\Delta INL_{max}(s=10) <$ 1LSB	6.9 %	12.0 %
$\{INL_{12}\}$ $\Delta INL_{max}(k=0) < 1$ LSB, $\Delta INL_{max}(s=10) <$ 1 LSB	8.2 %	13.6 %
$\{INL_{13}\}$ $\Delta INL_{max}(k=0) \cong 2$ LSB, $\Delta INL_{max}(s=10) <$ 1 LSB	4.8 %	9.8 %
$\{INL_{14}\}$ $\Delta INL_{max}(k=0) \cong 18$ LSB, $\Delta INL_{max}(s=10) < 1$ LSB	8.2 %	13.7 %

Tab.1 The designed correction architecture results by applying certain condition

The experiments show that the increasing length of the averaging windows 2^L (see Fig. 2 b)) and the increasing precision of the ET improve the accuracy of the measured system (see Fig. 2 a)). The triangular wave dither signal with the appropriate frequency (Eq. 1) and amplitude 2 LSB were used for the correlation breaking among the samples.

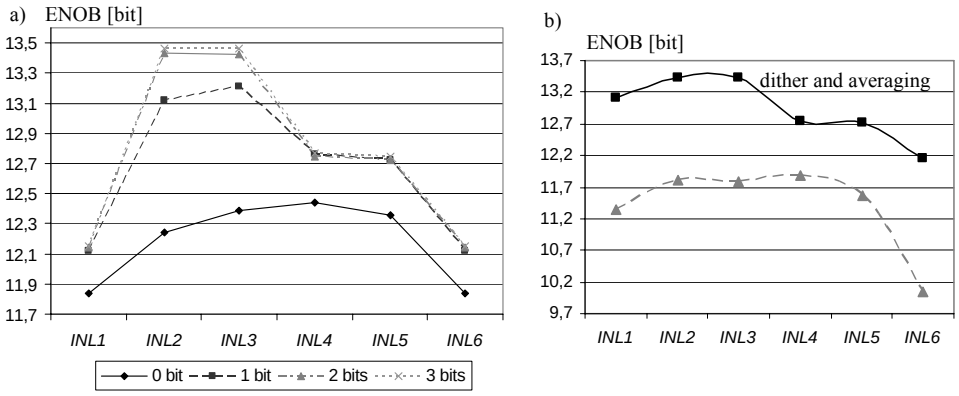

Fig. 2 a) The effect of increasing precision of the error table by 0 to 3 bit (see legend) and b) the increasing amount of averages windows 2^2 samples together with triangular wave dither with the amplitude 2 LSB

The contribution of the slope calculated by the Wiener filter in the addressing depends on the INL shape. The influence of the ET address reduction on the ENOB is being studied for ADC with the particular INL_1 phase plane (Fig. 3 a)). As mentioned before, the error table is represented by the median value in the centre of the adjacent 2^k cells along code axes and 2^s cells along slope axes. Fig. 3 b) shows the ENOB after ET correction with precision after decimal point β=2 bit and averaging with 2^5 long window of the ADC with original ENOB = 7.6 bits.

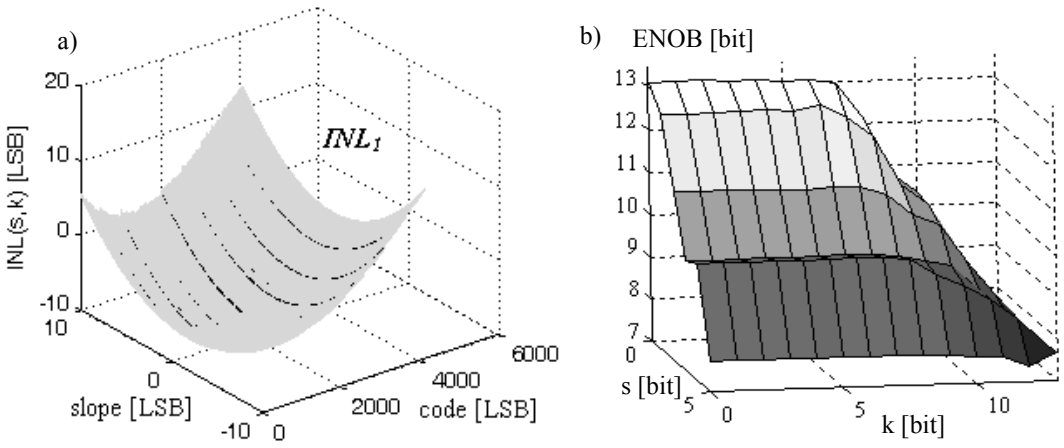

Fig. 3 a) The two dimensional INL_1 and b) the results of a designed algorithm application on the error table compressed by 2^k code cells and 2^s slope cells

The *INL* characteristic must meet certain conditions to be effective for dynamic correction by two dimensional ET. The simulations show that for the *INL* change in *s* axes $\Delta INL_{max}(k=0) \leq 1\ LSB$ corresponding to the slope difference Δs=20 the correction using code *k* is sufficient (Fig. 4, Tab. 1).

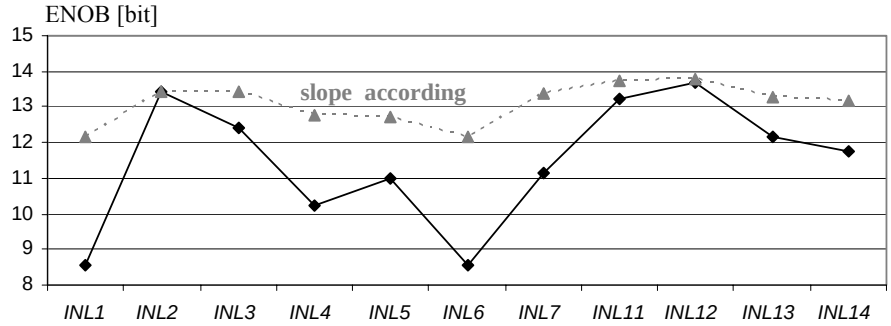

Fig. 4 The comparison of the slope according algorithm and non slope according algorithm

The simulation results were verified by experimental tests. The input limiter on the (Fig. 5 a) determines the final *INL* curve with *12 bit* ADC with neglected *INL*. The *INL* shape of the whole data acquisition block is shown in Fig. 5 b).

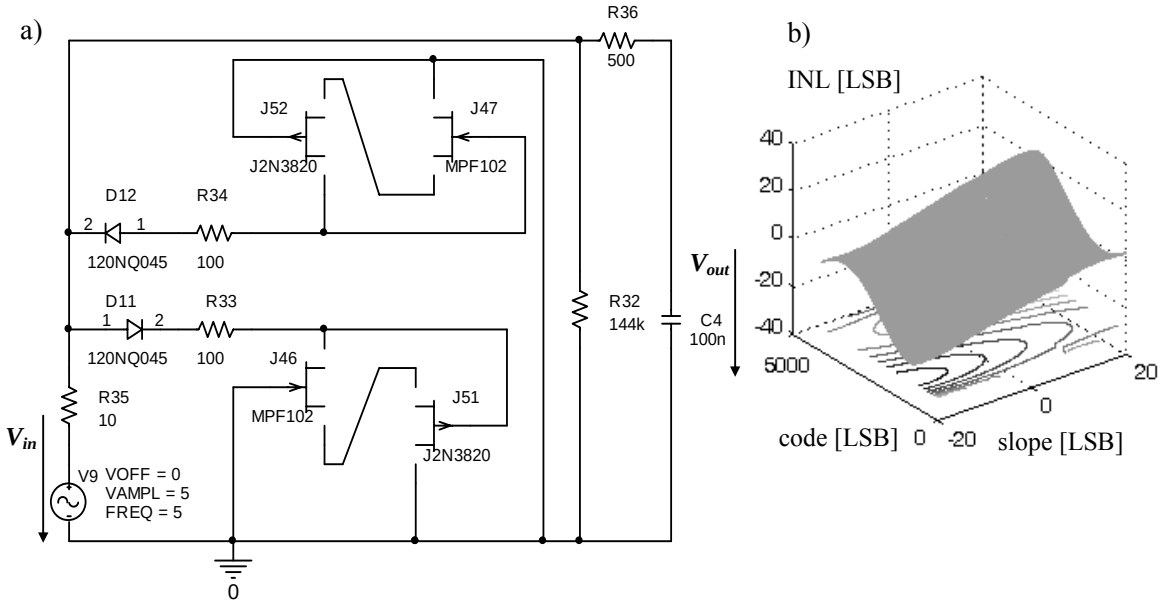

Fig. 5 a) The scheme designed for analogue INL modelling and b) the modelled INL

4 CONCLUSION

The paper presented the correction algorithm based on the error table correction and dithering. The simulation results show that the low code frequency component of integral nonlinearity (^{LCF}INL) is reduced mainly by the ET and high code frequency part (^{HCF}INL) by dithering and averaging. The dynamic correction using slope information for ET significantly improves correction for the maximal error change s $\Delta INL_{max}(k=0) \geq 1LSB$.

The proposed correction method is useful for generalised AD interface with the significant error contribution caused by the analogue preprocessing block. The dynamic error is notable for the harmonic signal with the frequency close to the high frequency limit.

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