

Hardware Prototyping of Neural Network based Fetal Electrocardiogram Extraction

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The aim of this paper is to model the algorithm for Fetal ECG (FECG) extraction from composite abdominal ECG (AECG) using VHDL (Very High Speed Integrated Circuit Hardware Description Language) for FPGA (Field Programmable Gate Array) implementation. Artificial Neural Network that provides efficient and effective ways of separating FECG signal from composite AECG signal has been designed. The proposed method gives an accuracy of 93.7% for R-peak detection in FHR monitoring. The designed VHDL model is synthesized and fitted into Altera's Stratix II EP2S15F484C3 using the Quartus II version 8.0 Web Edition for FPGA implementation.

Keywords: Fetal electrocardiogram, neural network, FPGA, VHDL

1. INTRODUCTION

TO MONITOR fetal status, the fetal heart rate (FHR) analysis has become a widely accepted technique. The physician or clinician could identify problems in FHR activity during the pregnancy if they could obtain a reliable reading of the FECG. The FECG is a biomedical signal that can be obtained non-invasively from the abdomen of a pregnant woman by employing a set of electrodes [1]. The prominent attributes of the FECG signal, such as presence of signal, magnitude or frequency, wave shape and dynamic behavior are useful for specifying the fetal lifespan, fetal maturity and being of fetal distress or inborn heart disease. Thus, the demand for the powerful and advanced methodologies for extraction of FECG signals from the AECG signal is strongly rising in biomedical engineering. However, the FECG signal is susceptible to noise, thus, an analysis of efficient processing is necessary to remove the noise in the AECG signals [1]. The recording of AECG is associated with the number of difficulties and complication steps. The AECG contains a weak FECG signal, a comparatively sound MECG, maternal muscle noise (electromyographic activity in the muscles of the abdomen and uterus), thermal noise from the electronic equipment (electrodes, amplifiers, etc.), and power line interference (A/C) [2]. The signal processing algorithm serves to enhance the FECG signal for FHR monitoring effectively by removing MECG, reducing the effects of motion artifact, muscle noise and power line interference. The most dominant interfering signal is MECG which is found with FECG in the abdominal signal [3]. The frequency spectrum of each noise source partially overlaps with FECG in the AECG signal and hence, filtering alone is not adequate to achieve tolerable noise reduction. Techniques to get better FECG acquisition from AECG signal remain the subject of ongoing research these days. Up to date progress in technologies of signal processing approach and mathematical framework has made it straightforward to develop advanced FECG extraction and analysis techniques

[4]. Ranges of mathematical techniques and Artificial Intelligence (AI) have noticed a comprehensive attraction for FECG extraction [5-8]. Moreover, independent component analysis approaches have also been applied and developed on embedded processor for extracting the FECG from AECG signal [9]. Methods for extracting abdominal FECGs have been recently introduced for remote monitoring of the FHR [10]. So far, research and extensive effort have been formed in the area for developing better algorithms, elevating current methodologies to reduce noise and acquire accurate FECG from AECG signal. Therefore, reliable information about the fetus state can assure the fetus' well-being during the pregnancy period.

The main purpose of this research work is to develop and design an AI method to extract FECG from AECG signal that could be used in a compact and portable FECG extraction system. Here, Neural Network is applied to model a portable hardware system using VHDL language for an efficient FECG extraction. The designed VHDL model could be loaded into the FPGA for intermediate physical realization. Neural Network has been primarily chosen as it is adaptive to the nonlinear and time-varying features of ECG signal. The predicted MECG is considered as the input and the AECG is considered as target signal for the network. Using this Neural Network approach, the MECG is suppressed efficiently from the AECG by correlation detection, so that the output can be considered as FECG only.

2. METHODOLOGY

The architecture of the neural network is designed mainly by using the adaptive filtering approach that is the combination of ADALINE (adaptive linear network) and TDL (tapped delay line) which was described in detail in our previous work [11] shown in Fig.1. Our previous work was mainly on the signal processing algorithm for FECG extraction only but this article is about the hardware prototyping of that algorithm. ADALINE has been

considered in our study mainly as one of the robust filtering techniques that use a Neural Network topology and which proved to be one of the best adaptive filtering algorithms [12]. According to the concept of TDL, the MECG signal enters and passes through the N-1 delays and the output of the TDL is an N-dimensional vector, made up of the input signal at the current time, the previous signal that is fed to the ADALINE.

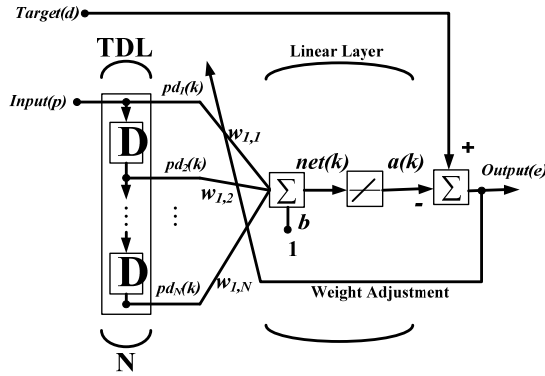


Fig.1. Adaptive Filter Network [11]

The MECG, which is predicted and close to the AECG, passes through the one $(N - 1, \text{ where } N = 2)$ tapped delay line. The tapped delay line was considered mainly due to lower complexity and modeling of FPGA. The delayed output was multiplied by the two corresponding initial weights. The initial weight was considered $w_{1,1} = 0$, and $w_{1,2} = -2$. After adding the weighted output, it passes through the linear activation function. Finally, the output of the network was detracted from the AECG signal to reduce the difference between input and target signal; the weights were updated in every step. Therefore, the difference is considered as FECG signal. The input (MECG) is considered as p , the target signal (AECG) is considered as

d and the adaptive weight is considered as w . The

learning rate is η and the momentum is m . To get the maximum satisfactory fetal ECG output, the optimal learning rate was 1 and momentum value was 0.2. Therefore, the network representation can be written as:

$$net_{\rightarrow} = w \cdot p \quad (1)$$

$$a_{\rightarrow} = g(net_{\rightarrow}) = net_{\rightarrow} \quad (2)$$

$$\delta_{\rightarrow} = d_{\rightarrow} - a_{\rightarrow} \quad (3)$$

The learning rule is:

$$w_{new} = w_{old} + (1 - m)\eta \cdot \delta_{\rightarrow} \cdot p \quad (4)$$

Initially, the custom designed MATLAB® program was used to extract the FECG signal because it was simpler and faster to verify the functionality and reliability for the designed algorithm. After performing the efficient FECG extraction from AECG using MATLAB tools, the whole algorithm was designed using VHDL language; where Altera's Quartus II version 8.0 Web Edition was used as the platform. As a result, VHDL implementation of the algorithm has to be perceived as a structural, behavioral and physical version of the algorithm. The design flow of the entire algorithm for hardware prototyping for this research is shown in Fig.2.

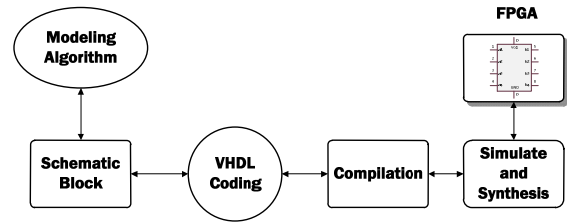


Fig.2. Hardware Modeling for FPGA implementation

The initial modeling of the FECG extraction algorithm has been designed. The second step of the implementation has been considered by considering the schematic block diagram and then VHDL coding was done. The software Quartus II Web Edition has been used and the code has been simulated functionally and synthesized for FPGA implementation. The advantage of using Quartus II is that the designed model could be synthesizing the system into a physically available FPGA [13]. The top entity of the overall VHDL model comprises three inputs - Clock, AECG and MECG and one output - FECG. Fig.3 shows the four different modules of VHDL model, which are ReadData, Preminmax, Neural Network and Postminmax. These four modules have been considered to simplify the total implementation of Neural Network into the hardware system. Through these modules the Neural Network algorithm has been implemented.

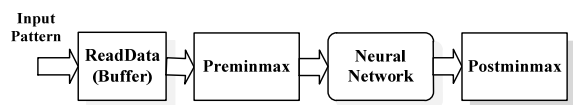


Fig.3. Block diagram of four modules

The part of the flow of VHDL implementation for functional simulation is shown in Fig.4. This part describes mainly how the biomedical (AECG, MECG and FECG) signal can be processed for real-time FPGA implementation by following the procedure of hardware prototyping. The input signal for the system was taken from the vector waveform file in each positive clock edge and simulated into functional simulation behavior shown in Fig.4.

The main inputs, AECG and MECG, are given through the ReadData module using the clocked input concept. For every positive edge of the clock, each sample point of the AECG and MECG is read by using the ReadData module. Before feeding the inputs into the Neural Network module, all inputs are normalized by using the Preminmax module.

After normalizing, all inputs are passed to the next module - Neural Network. In the Neural Network module, the ADALINE is implemented to process all the normalized inputs and finally the output of the Neural Network module is de-normalized using the last module, Postminmax, to get the actual value of the outputs (FECG).

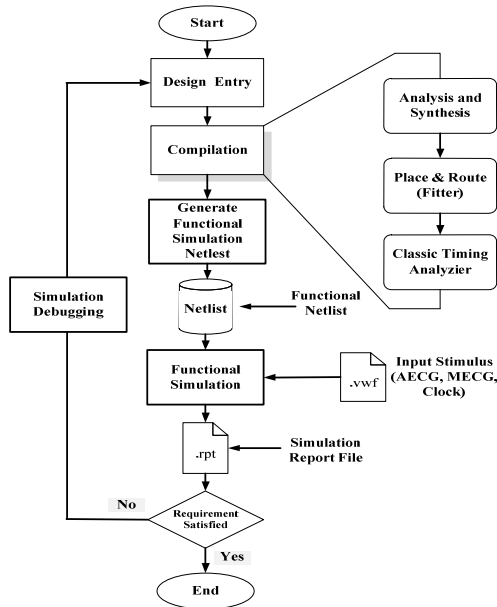


Fig.4. Flow chart for VHDL implementation

6. RESULTS AND DISCUSSION

The recorded signals are downloaded from MIT/BIH PAF Prediction Challenge database website in binary format. In this study, 10-recorded signals have been investigated. The obtained signals consisted of both normal AECG and AECG with paroxysmal atrial fibrillation. C++ program was used to convert these results manually to text file format *.txt. Since the total number of samples was large (128 samples per second = 7680 samples per minute, thus total samples = 7680*40 = 307200 samples per subject), only two thousand samples were converted in each text file (2000*4 = 8000 samples per subject). This served to reduce the neural network training time. The algorithm has been examined using several AECG signals. One of the tested signals is shown in Fig.5. According to the figure, M denotes the peak of maternal QRS and F denotes the peak of fetal QRS complex from AECG signal. In this figure, the AECG signal contains the MECG and FECG. Our developed algorithm is able to extract FECG from the AECG completely. In the figure, around 700 ms in AECG signal, QRS complex of FECG and MECG are overlapped. It is clearly shown in the figure that the designed algorithm is extracting the FECG from the AECG even in the overlapping QRS portion of MECG and FECG. Learning constant and momentum affect the FECG signal after its extraction from the AECG [14]. In this figure, first 100 ms data, the QRS complex of FECG is not clear like the ordinary QRS complex; however, by changing the learning rate and momentum value, it is possible to obtain a regular QRS complex. From this figure, it can be said that the FECG signal is extracted efficiently from the AECG signal.

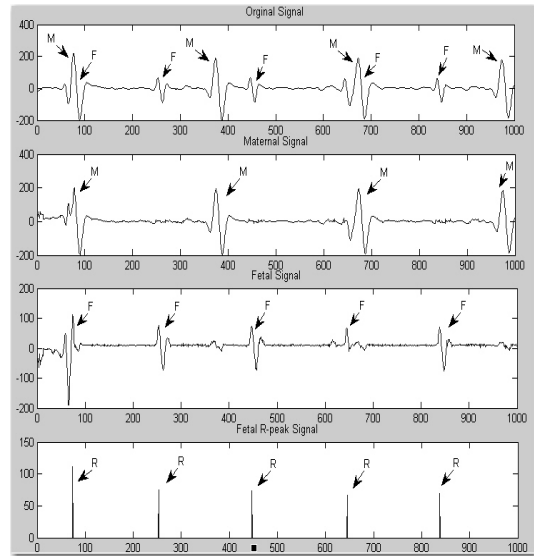


Fig.5. Suppressed fetal ECG from abdominal ECG to maternal ECG [11]

In order to analyze detection performances of the detection scheme, specific sets of AECG signals were tested by using the performance measurement equation [15].

$$Performance = \frac{\# fetal R wave - (\# miss + \# false)}{\# fetal R wave} \times 100 \quad (5)$$

The performance of the proposed method for R-peak detection in FHR monitoring was 93.75%.

In hardware modeling initially all the inputs were multiplied by 1000 to make the final VHDL simulation output (wave form) simple and to avoid the unnecessary floating-point calculation. Floating point calculation in VHDL is a tedious and complex task. VHDL synthesizes only the real number and cannot represent the floating-point value in the simulation waveform output. After the final simulation, the output was computed by dividing 1000 so that the output can be similar to the real output of MATLAB simulation. The compilation summary report of the synthesis is shown in Table1, where logic utilization is 36%, and the total number of resistors used is 1721.

Table 1. Compilation Summary

Entity	Description
Top Entity Name	Fetal
Family Name	Stratix
Device Name	EP2S15F484C3
Combinational ALUTs	4458
Dedicated logic registers	1721
DSP block 9-bit elements	56
Logic Utilization	36%
Total Number Register	1721
Total Number of Pins	153

Fig.6 shows a part of the simulation result. In the simulation output, the AECG, CLOCK, FECG and MECG value are marked by a circle. In this figure, the FECG values are -5015, -6096, -33669, -36577, 8572, -4521, -3030, -

5676, -5613, 8866, -7850, 2053. After dividing these values by 1000 the result becomes -5.015, -6.096, -33.669, -36.577, 8.572, -4.521, -3.030, -5.676, -5.613, 8.866, -7.850, 2.053 where the simulation result from the MATLAB tools is -5.00, -6.08, -33.67, -36.59, -32.71, 8.52, -4.50, -3.026, -5.66, -5.59, 8.86, -7.88, 2.05. Therefore, it can be said that the designed hardware model using VHDL language is accurate for extracting FECG from the AECG signal.

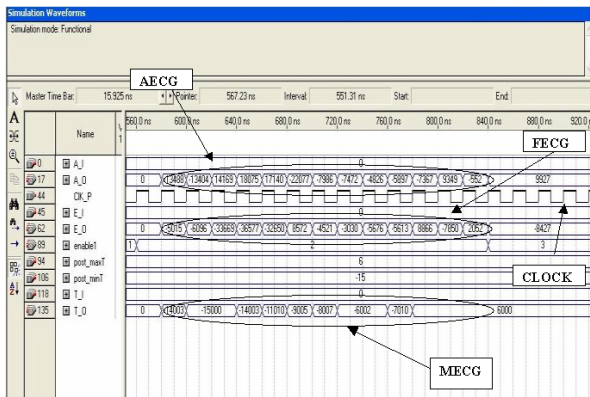


Fig.6. A sample simulation result of FECG extraction (VHDL)

7. CONCLUSION

The ADALINE approach is applied to extract the FECG from the AECG signal. In fact, the accuracy of the designed algorithm depends on the variations of testing signals that are used as input and the target signal in the network. The performance of the designed model is quite high and satisfactory. In addition, Hardware Description Language (HDL) is used to model the proposed algorithm for hardware prototyping by implementing in Stratix II FPGA from Altera, which will make the FHR monitoring system compact and portable. Thus, the long term FHR monitoring can be possible in proficient and effectual way to give utmost benefits to the pregnant women and fetus during the pregnancy.

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