MEASUREMENT SCIENCE REVIEW, **17**, (2017), No. 3, 100-107

DE GRUYTER OPEN

MEASUREMENT SCIENCE REVIEW

Journal homepage: http://www.degruyter.com/view/j/msr

ISSN 1335-8871

# New Discrete Fibonacci Charge Pump Design, Evaluation and Measurement

David Matoušek[1], Jiří Hospodka[1], Ondřej Šubrt[2, 1]

[1]*Department of Circuit Theory, FEE CTU in Prague, Technicka 2, 16627, Prague, Czech Republic, matoudav@fel.cvut.cz*
[2]*ASICentrum, a company of the Swatch Group, Novodvorska 994, 14221, Prague, Czech Republic*

This paper focuses on the practical aspects of the realisation of Dickson and Fibonacci charge pumps. Standard Dickson charge pump circuit solution and new Fibonacci charge pump implementation are compared. Both charge pumps were designed and then evaluated by LTspice XVII simulations and realised in a discrete form on printed circuit board (PCB). Finally, the key parameters as the output voltage, efficiency, rise time, variable power supply and clock frequency effects were measured.

Keywords: Dickson charge pump, Fibonacci charge pump, voltage gain, output series resistance, rise time, efficiency.

## 1. INTRODUCTION

Charge pumps are DC/DC converters that produce a voltage higher than supply voltage or a negative voltage. Charge pumps are suitable for a lower value of the output current and take advantage of having no inductive storage elements, whereas, conventional DC/DC converters based on inductors or transformers are more suitable for a higher power. A standard variant of a charge pump is the Dickson charge pump. The Dickson charge pump is efficient, but it produces a relatively small voltage gain. Thus, the Dickson charge pump is useful for lower output to input voltage ratios. A Fibonacci charge pump is a charge pump variant with the voltage gain that is gradually increased over pump stages. On the other hand, the Fibonacci charge pump circuit is more complex than the Dickson charge pump circuit solution.

The Dickson Charge Pump (DCP) is a well-known variant of a charge pump [1]. The schematic diagram is shown in Fig.1. The design equations for DCP are summarised in [2].

The differential voltage $\Delta V$ between nodes $n$ and $n+1$ is

$$\Delta V = V_{n+1} - V_n = V_S - V_D, \tag{1}$$

where $V_S$ is the voltage swing at each node due to capacitive coupling from the clock [2], $V_D$ is the diode forward voltage.

The optimal value of the voltage swing equals to the amplitude of clock. But the stray capacitance of a node reduces voltage swing [1] as follows

$$V_S = \left(\frac{C_T}{C_T + C_S}\right) \cdot V_{CLK}, \tag{2}$$

where $V_S$ is the voltage swing, $C_T$ is the transfer capacitance, $C_S$ is the stray capacitance, $V_{CLK}$ is the amplitude of clock.

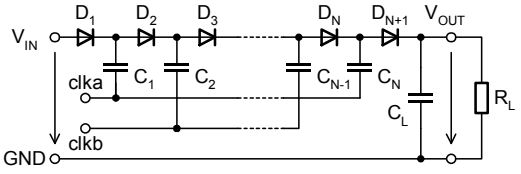


Fig.1. Schematic diagram of the Dickson Charge Pump.

The no-load output voltage applies here according to [1]

$$V_O = V_{IN} + N \cdot (V_S - V_D) - V_D, \tag{3}$$

where $V_O$ is the no-load output voltage, $V_{IN}$ is the input voltage, $N$ is the number of stages, $V_S$ is the voltage swing, $V_D$ is the diode forward voltage drop.

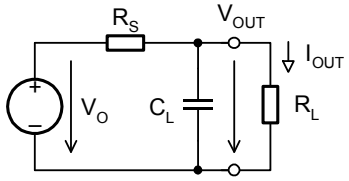


Fig.2. The equivalent circuit of DCP.

The equation (3) assumes the no-load output. The effect of the load current is described by [1] (see Fig.2.).

DOI: 10.1515/msr-2017-0013

$$V_{OUT} = V_O - I_{OUT} \cdot R_S, \tag{4}$$

where $V_{OUT}$ is the output voltage at load, $V_O$ is the no-load output voltage, $I_{OUT}$ is the load current ($I_{OUT} \geq 0$), $R_S$ is the output series resistance of the charge pump.

Reference [1] defines the output resistance of the charge pump as the dependency on the number of stages $N$, transfer capacitance $C_T$, stray capacitance $C_S$ and clock frequency $f$

$$R_S = \frac{N}{(C_T + C_S) \cdot f}. \tag{5}$$

The validity of (5) is limited by the finite resistance of the diodes in use and also the finite output resistance of clock drivers for generating clka and clkb signals [3]. Equation (5) assumes that influence of the resistance of diodes and clock drivers is sufficiently small in the relationship with the equivalent resistance of the transfer capacitors. This condition is usually granted for a low capacitance of the transfer capacitors. But for relatively high values of the transfer capacitance, (5) becomes invalid.

## 2. SUBJECT & METHODS

The design of the Dickson charge pump and the Fibonacci charge pump was carried out and evaluated by simulations.

### *A. DCP design and evaluation*

The design rules for DCP are summarised in [2] and illustrated by Fig.3. We assume these charge pump specifications:

- power supply voltage $V_{IN} = 3$ V,
- the minimal steady-state output voltage $V_{OUT} = 30$ V at the output current $I_{OUT} = 1$ mA,
- the maximal ripple voltage of the output $V_R = 15$ mV,
- the maximal rise time of the output $t_R = 65$ ms.

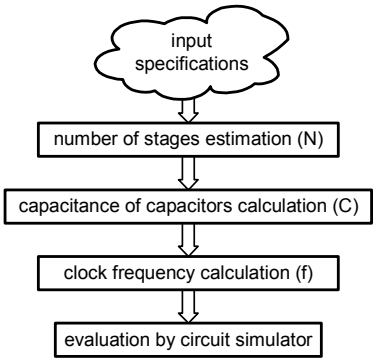


Fig.3. Design-flow diagram.

At first, the number of stages of the Dickson charge pump was estimated by (3) and (4). Ideally, we assume $V_S = V_{IN}$, $V_D = 0$, $R_S = 0$ then the required number of stages is (6). Thus, the number of stages estimation is $N = 9$. As it is evident, the number of stages must be increased. We set $N = 11$.

$$N = \frac{V_{OUT}}{V_{IN}} - 1, \tag{6}$$

Secondly, the capacitance of capacitors was calculated from known values of the output voltage and current and required rise time of the output (7) [2]. The calculated value is used for the transfer and load capacitors ($C = C_T = C_L$). We calculate $C = 2.17$ μF and then we set $C = 2.2$ μF.

$$C = \frac{I_{OUT} \cdot t_R}{V_{OUT}}, \tag{7}$$

where $C$ is the load and transfer capacitance, $V_{OUT}$, $I_{OUT}$, $t_R$ are the voltage, current, and rise time of the output.

As the third step, the clock frequency was calculated from known values of the output current, output ripple voltage, and load capacitance (8) [1]. We calculate $f = 30.3$ kHz and then we set $f = 33$ kHz.

$$f = \frac{I_{OUT}}{V_R \cdot C_L}, \tag{8}$$

where $f$ is the clock frequency, $I_{OUT}$ is the output current, $V_R$ is the ripple voltage of the output, $C_L$ is the load capacitance.

Finally, we select the transistors and diodes. All design parameters are listed in Table 1.

Table 1. Input design parameters and result device parameters.

| **Parameter** | **Value or device** |
|---|---|
| Output voltage | $V_{OUTmin} = 30$ V ($I_{OUT} = 1$ mA). |
| Rise time of output | $t_{Rmax} = 65$ ms. |
| Ripple voltage | $V_{Rmax} = 15$ mV. |
| Clock frequency | $f = 33$ kHz. |
| Supply voltage | $V_{IN} = 3$ V. |
| Capacitances | $C_L = C_T = 2.2$ μF. |
| NMOS transistor | 2N7002 ($V_{DSS} = 60$ V, $V_{GS(th)} = 2.1$ V). |
| PMOS transistor | BSS84 ($V_{DSS} = -50$ V, $V_{GS(th)} = -1.7$ V). |
| Schottky diode | PMEG4010BEA ($V_{RRM} = 40$ V, $V_D = 155$ mV). |

The final DCP schematic diagram is shown in Fig.4. This circuit solution uses one common clock signal CLK only. The clock signals clka and clkb are derived from the CLK by two inverters $M_1$, $M_2$ and $M_3$, $M_4$. Thus, these clock signals are overlapped. This solution is easier than a generation of non-overlapped clock signals. At this point, overlapping is not a key factor for the DCP function (this phenomenon does not kill the DCP voltage gain).

The proposed DCP was simulated in LTspice XVII from Linear Technology Corporation. Results from simulations are the output no-load voltage $V_O = 34.90$ V and output voltage $V_{OUT} = 32.78$ V at load ($I_{OUT} = 1$ mA). The rise time of the output is $t_R = 37.07$ ms, and the ripple voltage of the output is $V_R = 7.23$ mV (p-p).

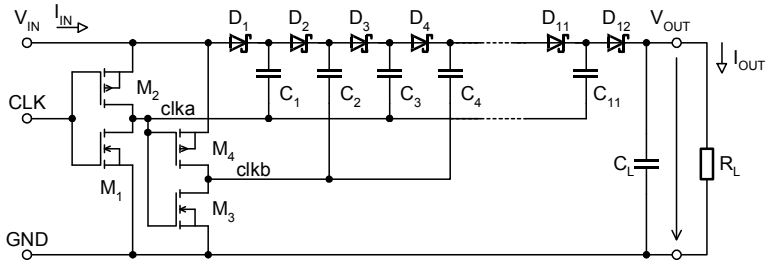


Fig.4. Schematic diagram of the 11-stage DCP.

*B. Fibonacci Charge Pump principles*

Fibonacci Charge Pump (FCP) [4], [5] is a voltage multiplier with a gradually increasing voltage gain of the stages. The voltage gain of the stage is defined as a Fibonacci number (the Fibonacci sequence is: 1, 1, 2, 3, 5, 8, 13, 21, …).

Schematic diagram of the Fibonacci charge pump is shown in Fig.5.

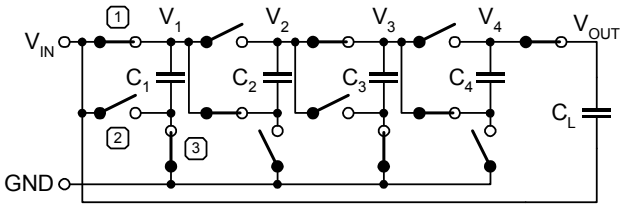


Fig.5. Schematic diagram of the 4-stage Fibonacci charge pump.

The voltages of the individual nodes $V_1$ to $V_4$ in periodic steady-state are gradually shifted about multiple of the voltage gain of the first stage. Thus, the 4-stage FCP produces the no-load output voltage $V_O = V_{IN} + 7 \cdot V_{IN}$. Generally, the no-load output voltage $V_O$ is

$$V_O = V_{IN} + V_{IN} \cdot \sum_{n=1}^{N} F_n , \tag{9}$$

where $N$ is the number of stages, $F_n$ is the Fibonacci number of the nth order ($F_1 = 1$, $F_2 = 1$, for $n \geq 3$: $F_n = F_{n-1} + F_{n-2}$).

The effect of the load current is similar as in DCP and it is described in Fig.2. and by the equation (4). The output series resistance of FCP is discussed in [6].

*C. Proposed FCP realisation*

For a given case according to Table 1., the number of FCP stages must be set to N = 5, because the ideal no-load output voltage for the 5-stage FCP is $V_O = 39$ V. A lower value of the number of stages is not sufficient (e.g. for N = 4 the no-load output voltage is $V_O = 24$ V only) because the required output voltage at the load is 30 V minimally. The values and types of devices according to Table 1. are unchanged for FCP realisation. Thus, we can compare key parameters of DCP versus FCP.

Realisation of the Fibonacci charge pump is more complicated than the Dickson charge pump circuit solution.

The key problem is that FCP uses two floating switches for each stage. For the first stage from Fig.5. these switches are marked as 1 and 2. The switch #1 can be realised as a diode, but the switch #2 must be realised as a transistor. This high-side switch must be realised as a PMOS transistor. This solution is more suitable than driving an NMOS high-side switch. The switch #3 can be realised as an NMOS transistor that works as a low-side switch. To summarise, the switches for the first stage are realised by diode $D_1$ (switch #1), transistor $M_{1b}$ (switch #2) and transistor $M_{1a}$ (switch #3), see Fig.6.

The second problem of FCP realisation is generating of a driving signal for the switches #2 and #3 for the next stage. A driver for the next stage must be supplied from the output of a current stage and inverts a clock signal to the next stage. The optimal solution of this problem is an auxiliary inverter [7] that is supplied from the output of a current stage and driven from the clock signal of a current stage. This inverter generates inverted and voltage shifted clock signal for the next stage. For example, the second stage of FCP is driven by inverter $M_{1c}$, $M_{1d}$, see Fig.6.

The presence of the auxiliary inverter implies the fact that a shoot-through current arises. The intermediate nodes are discharged by this shoot-through current. Thus, the power consumption is increased. This problem may be solved by a more complex architecture of the inverter with an auxiliary current limiter.

The second problem of the implemented auxiliary inverter is the propagation delay. The propagation delay of inverters is gradually increased from the input to the output of the charge pump. The timing discrepancy between the stages may cause a loss of a charge. Thus, the clock period should be set sufficiently long related to this propagation delay.

Proposed new circuit solution of FCP according to Fig.6. was verified by simulation in LTspice XVII. Results from simulations are the output no-load voltage $V_O = 35.00$ V, output voltage $V_{OUT} = 33.14$ V at load ($I_{OUT} = 1$ mA), rise time of the output $t_R = 17.37$ ms, and ripple voltage of the output $V_R = 7.24$ mV (p-p).

The question of an optimal value of the clock frequency is very important in a relationship with the above-mentioned influence of the shoot-through current. The capacitance C = 2.2 μF and the frequency f = 33 kHz calculated from (7) and (8) were used as a reference design. Both these parameters were proportionally changed to values: C = 1 μF and f = 73.3 kHz, C = 4.7 μF and f = 15.6 kHz, C = 10 μF and f = 7.33 kHz. The simulation results are presented in Fig.7.

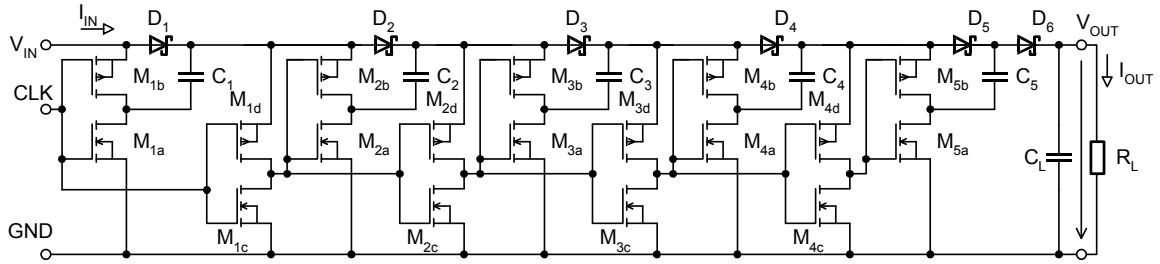


Fig.6. Schematic diagram of the 5-stage FCP.

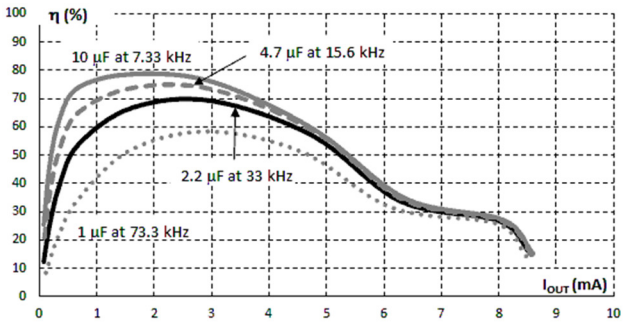


Fig.7. Efficiency vs. output current for various values of capacitance of capacitors.

The increase of the clock frequency by two times approx. to f = 73.3 kHz causes a significant decrease of the efficiency at low values of the output current, whereas, the clock frequency decrease causes the efficiency boosting. The reference design (C = 2.2 µF and f = 33 kHz) was used as a compromise between the efficiency and capacitors values.

## 3. MEASUREMENT PROCEDURE AND RESULTS

Proposed 11-stage Dickson charge pump (see Fig.4.) and 5-stage Fibonacci charge pump (see Fig.6.) were realised from discrete devices that are listed in Table 1. The realised PCBs contain five terminals for connecting the input voltage $V_{IN}$, output voltage $V_{OUT}$, GND (ground), and the clock signal (see Fig.8.).

Fig.8. shows PCB samples of the first realisation of the proposed DCP and FCP. These samples were realised as single-sided PCBs. The second realisation of DCP and FCP were implemented as double-sided PCBs. The 11-stage DCP had dimensions 42.55 × 11.91 mm. The 5-stage FCP had dimensions 40.32 × 12.38 mm.

The key parameters of both charge pumps were measured by the circuit according to Fig.9. The ammeters $A_1$ and $A_2$ measure the input and output currents. The input current corresponds to the consumed current, and the output current corresponds to the current of a load. The voltmeters $V_1$ and $V_2$ measure the input and output voltage. The used voltmeters had input resistances 20 MΩ.

We compensated a voltage drop of the ammeter $A_1$ in the time of the measurement. Thus, the input voltage was regulated to value $V_{IN}$ = 3 V accurately. The clock generator produced a square wave signal with frequency 33 kHz and voltage swing 0 to 3 V.

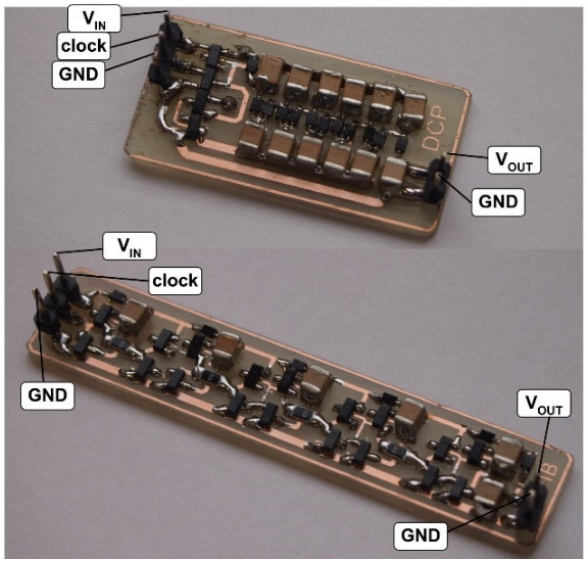


Fig.8. Photography of samples of the first realisation of DCP (top) and FCP (bottom).

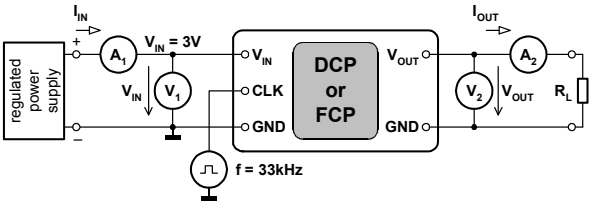


Fig.9. Schematic diagram of the measured circuit.

The FCP propagation delay from the clock input to the clock output of the last inverter ($M_{4c}$, $M_{4d}$, see Fig.6.) was 76 ns by the maximum. Thus, the measured value of the propagation delay is sufficiently small in comparison with the clock signal period (for frequency 33 kHz we get period 30 µs approx.).

### *A. Output voltage vs. output current*

The output voltage vs. output current characteristic is a relationship between the output voltage and the corresponding output current. The measured and simulated characteristics for the 11-order DCP and the 5-order FCP are shown in Fig.10.

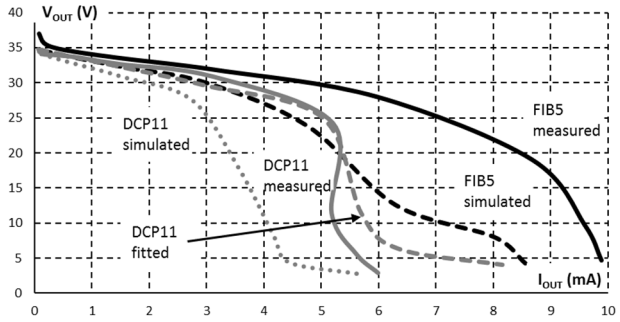


Fig.10. Output voltage vs. output current.

The measured characteristic of the 11-order DCP contains a region with negative differential resistance around $I_{OUT}$ = 5.3 mA (Fig.10., Fig.11., Fig.12., Fig.14., Fig.16.). This effect is caused by simplified construction of DCP clock drivers (see Fig.4.). The used clock drivers (inverters) are loaded by a relatively high capacitance and have not enough driving capacity. Moreover, the first inverter $M_1$, $M_2$ drives the second inverter $M_3$, $M_4$. The total load of the first inverter caused a significant increase of rising and falling edges of clka and decrease of the clka magnitude. Thus, the second inverter is not optimally driven. The described effect dominates especially at a higher value of the output current. Notice that due to the usage of discrete components, there was a slightly limited choice among MOS transistors. The inverters in the FIB pump are even a bit stronger than what is needed. On the other hand, adding more buffers to the DCP would penalize the efficiency of DCP – therefore we keep the DCP pump for simplicity as it is.

The difference between simulated and measured results is relatively high. This effect is predominantly caused by the threshold voltage variability of used transistors and diodes. The used transistors and diodes have a lower value of the threshold voltage than the value defined in simulated models.

The output series resistance $R_S$ for the output current $I_{OUT}$ = 1 mA can be calculated by [8]

$$R_S = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{V_{OUT2} - V_{OUT1}}{I_{OUT1} - I_{OUT2}}, \tag{10}$$

where $R_S$ is the output series resistance, $V_{OUT1}$ is the output voltage at the output current $I_{OUT1}$, $V_{OUT2}$ is the output voltage at the output current $I_{OUT2}$.

For the 11-stage DCP were measured values: $V_{OUT1}$ = 33.7 V at $I_{OUT1}$ = 0.714 mA, $V_{OUT2}$ = 32.7 V at $I_{OUT2}$ = 1.485 mA and calculated $R_S$ = 1.30 kΩ. For the 5-stage FCP were measured values: $V_{OUT1}$ = 34.4 V at $I_{OUT1}$ = 0.729 mA, $V_{OUT2}$ = 33.5 V at $I_{OUT}$ = 1.52 mA and calculated $R_S$ = 1.14 kΩ.

### *B. Efficiency vs. output current*

The efficiency of both charge pumps is calculated as the average output power to average input power ratio. The average value of the power is defined by [8]

$$P = \frac{1}{T}\int_0^T v(t) \cdot i(t) \cdot dt, \tag{11}$$

where $P$ is the average value of the power, $T$ is the period, $v(t)$, $i(t)$ are the voltage and current.

The used ammeters measure the average value of a current [9], and the input and output voltage in the steady-state are close to DC. Thus, the calculation of power can be simplified to form (12).

$$P = \frac{1}{T}\int_0^T v(t) \cdot i(t) \cdot dt = \frac{V}{T}\int_0^T i(t) \cdot dt = V \cdot I, \tag{12}$$

where $V$ is the DC voltage, $I$ is the average value of the current.

We calculated the efficiency by (13) from measured values of the ammeters and voltmeters.

$$\eta = \frac{P_{OUT}}{P_{IN}} \cdot 100\,\% = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} \cdot 100\,\%, \tag{13}$$

where $\eta$ is the efficiency, $P_{OUT}$, $P_{IN}$ are the average values of the output power and consumed power on input, $V_{OUT}$, $I_{OUT}$, $V_{IN}$, $I_{IN}$ are the measured values of voltages and currents.

The measured and simulated characteristics $\eta = f(I_{OUT})$ for the 11-order DCP and the 5-order FCP are shown in Fig.11.

The difference between simulated and measured results was caused by the threshold voltage variability of used transistors and diodes, again. The measured efficiency of FCP is higher than DCP over the all observed range of the output current.

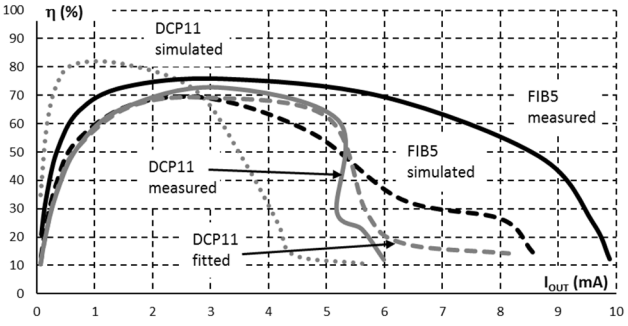


Fig.11. Efficiency vs. output current.

### *C. Output voltage and efficiency vs. output current for various input voltages*

The line regulation is an important characteristic of a charge pump. This characteristic corresponds to decreasing voltage of a system powered by batteries that are gradually discharged. The input voltage $V_{IN}$ was regulated to values 2.8 V, 2.9 V, and 3 V accurately. Simultaneously, the amplitude of clock was set to the same value as the input voltage. The load was set to $R_L$ = 30 kΩ.

The resulting characteristics from Fig.12. show that the output voltage of DCP is higher than the required value $V_{OUT}$ = 30 V at load $R_L$ = 30 kΩ. These values are 31.1 V, 31.7 V, 32.9 V.

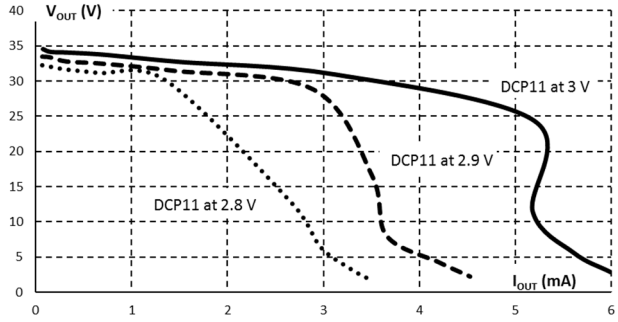


Fig.12. DCP output voltage vs. output current for various input voltages.

The resulting characteristics from Fig.13. show that the output voltage of FCP is higher than the required value $V_{OUT}$ = 30 V at load $R_L$ = 30 kΩ. These values are 31.2 V, 32.3 V, 33.8 V.

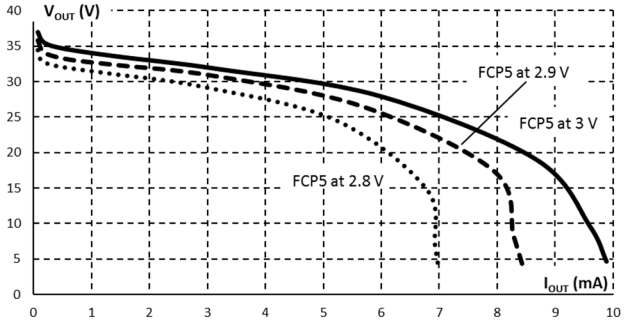


Fig.13. FCP output voltage vs. output current for various input voltages.

Secondly, the influence of the input voltage to the efficiency was measured, see Fig.14. and Fig.15.

The resulting efficiency characteristics of DCP from Fig.14. show that the efficiency for lower values of the output current is independent of the value of the input voltage. These characteristics are very similar up to the output current $I_{OUT}$ = 1.4 mA.

The resulting efficiency characteristics of FCP from Fig.15. show that the efficiency for lower values of the output current is independent of the value of the input voltage. These characteristics are very similar up to the output current $I_{OUT}$ = 3 mA.

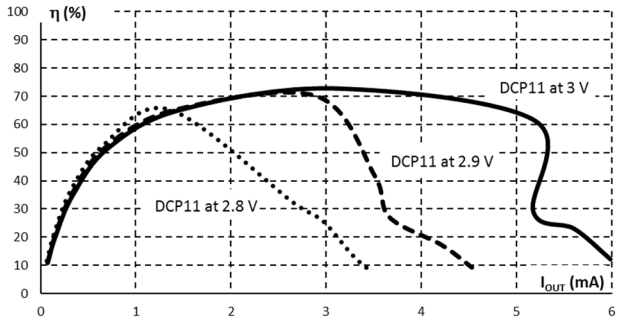


Fig.14. DCP efficiency vs. output current for various input voltages.

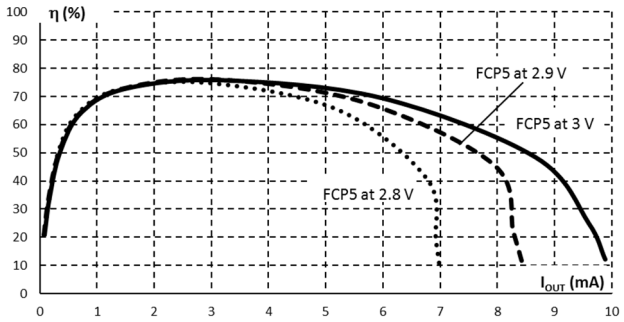


Fig.15. FCP efficiency vs. output current for various input voltages.

*D. Output voltage and efficiency vs. output current for various clock frequencies*

The clock frequency was subsequently set to values 10 kHz, 33 kHz, and 100 kHz.

The 11-stage DCP produced the output voltage at load $R_L$ = 30 kΩ, $V_{OUT}$ = 32.6 V, 32.9 V, 33.1 V for clock frequency 10 kHz, 33 kHz, and 100 kHz. Thus, the DCP conforms to the required value of the output voltage $V_{OUT}$ = 30 V at the output current $I_{OUT}$ = 1 mA.

The 5-stage FCP produced the output voltage at load $R_L$ = 30 kΩ, $V_{OUT}$ = 27.2 V, 33.8 V, 30.1 V for clock frequency 10 kHz, 33 kHz, and 100 kHz. Thus, the FCP conforms to the required value of the output voltage $V_{OUT}$ = 30 V at the output current $I_{OUT}$ = 1 mA except clock frequency 10 kHz.

The resulting efficiency characteristics of DCP from Fig.16. show that the efficiency for lower values of the output current is independent of the value of the clock frequency. These characteristics are very similar up to the output current $I_{OUT}$ = 2 mA.

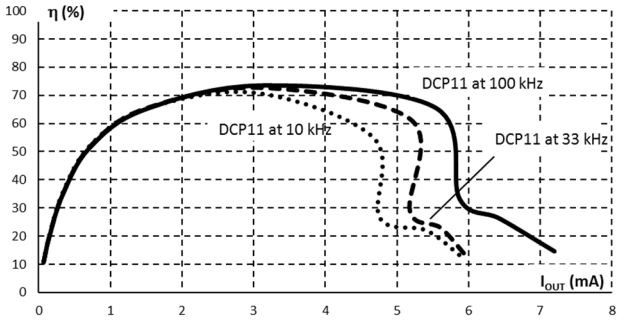


Fig.16. DCP efficiency vs. output current for various clock frequencies.

The resulting efficiency characteristics of FCP from Fig.17. show that the value of optimal clock frequency is 33 kHz. The efficiency is strongly dependent on frequency. At the lower frequencies, the FCP generates a lower output voltage. Thus, the efficiency has a lower value too (13). At the higher frequencies, the cross current of internal FCP inverters is increased. Thus, the input consumed current is increased too. The result is a lower value of the efficiency (13).

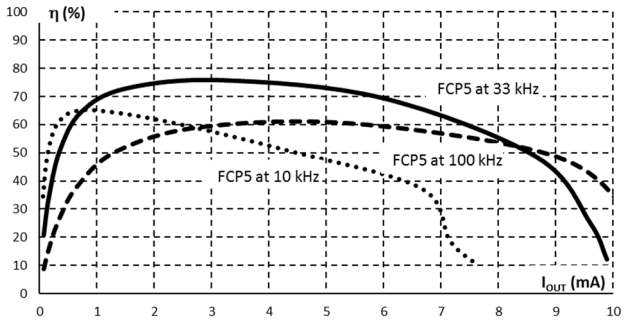


Fig.17. FCP efficiency vs. output current for various clock frequencies.

### *E. Rise time measurement*

The ramp of the output voltage was recorded by a digital oscilloscope in the arrangement depicted in Fig.18. The channel 1 was connected to the input and used as a synchronization source. The channel 2 was used for scanning of the output. The oscilloscope was configured for triggering by channel 1 and for a single shot. The oscilloscope recorded the ramp of the output voltage after closing the switch S.

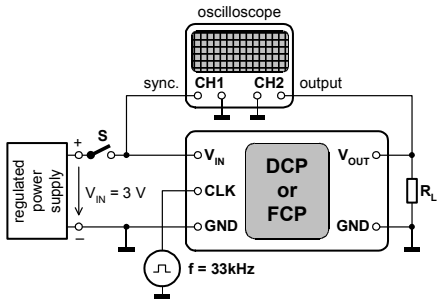


Fig.18. Schematic diagram of the CUT test bench.

These oscillograms were recorded for the load resistance $R_L$ = 30 kΩ. The used value of the load resistance implies the required minimal output voltage $V_{OUT}$ = 30 V at current $I_{OUT}$ = 1 mA.

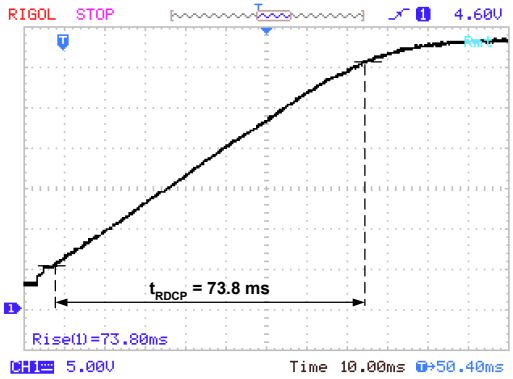


Fig.19. Oscillogram of the ramp of the DCP output at load $R_L$ = 30 kΩ.

Both charge pumps produced the steady-state output voltage higher than the required minimal value. The 11-stage DCP had the rise time $t_{RDCP}$ = 73.8 ms and the 5-stage FCP had the rise time $t_{RFCP}$ = 14.7 ms.

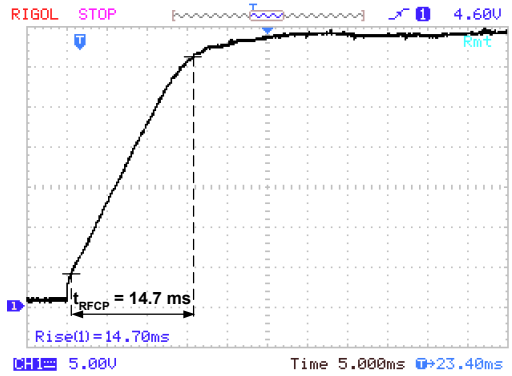


Fig.20. Oscillogram of the ramp of the FCP output at load $R_L$ = 30 kΩ.

## 4. RESULTS

The key parameters of the 11-stage Dickson charge pump and 5-stage Fibonacci charge pump are summarised and compared in Table 2.

Table 2. Comparison of simulated and measured results ($V_{IN}$ = 3 V, f = 33 kHz, $R_L$ = 30 kΩ).

| Parameter | DCP11 sim | DCP11 meas | FCP5 sim | FCP5 meas |
|---|---|---|---|---|
| $V_{OUT}$ | 31.7 V | 32.9 V | 32.6 | 33.8 V |
| η | 81 % | 60 % | 61 % | 69 % |
| $R_S$ | 2.24 kΩ | 1.30 kΩ | 1.58 kΩ | 1.14 kΩ |
| $t_R$ | 45.3 ms | 73.8 ms | 17.9 ms | 14.7 ms |
| $V_{Rp-p}$ | 7 mV | 11 mV | 7 mV | 10 mV |
| $N_C$ | 12 | 12 | 6 | 6 |
| $N_D$ | 12 | 12 | 6 | 6 |
| $N_T$ | 4 | 4 | 18 | 18 |

*DCP11sim*, *DCP11meas* mean the results from simulation or measurement of DCP, *FCP5sim*, *FCP5meas* mean the results from simulation or measurement of FCP, $V_{IN}$, $V_{OUT}$ are the input and output voltages, $f$ is the clock frequency, $R_L$ is the load resistance, $\eta$ is the efficiency, $R_S$ is the output series resistance for output current 1 mA, $t_R$ is the rise time of the output, $V_{Rp-p}$ is the peek-to-peek ripple voltage of the output, and $N_C$, $N_D$, $N_T$ are the required number of capacitors, diodes, and transistors.

Compared to DCP, the extra costs on FIB could potentially allow making a high-performance CP eliminating effectively the number of capacitors in the design. Notice that low loss capacitors could be expensive components. This fact, together with a limited number of low loss capacitors, tends to achieve much higher efficiency.

## 5. CONCLUSION

In this article, a circuit solution compact implementation of the Fibonacci pump was presented, including the detailed design procedure considering an improved clock buffer scheme.

The key parameters of the Dickson charge pump and the Fibonacci charge pump were simulated and then measured. Some differences between simulations a measurement are evoked by a variability of parameters of used devices. E.g. variability of the threshold voltage of used transistors or forward drop voltage of used diodes has a strong effect on many observed parameters. The diode and transistor threshold voltage spread was taken into account by post-fitting of the device model parameters. The reverse bias saturation current and the series resistance of the diode model were changed to values $I_S = 600$ μA and $R_S = 0.1$ Ω (original values: $I_S = 2.831$ μA and $R_S = 0.1975$ Ω). The threshold voltage of NMOS transistor model was changed to value $V_{T0} = 1.5$ V (original value: $V_{T0} = 1.6$ V). The threshold voltage of PMOS transistor model was changed to value $V_{T0} = -1.5$ V (original value: $V_{T0} = -2.1$ V). Fig.10. and Fig.11. show the results from simulations after fitting models of used transistors and diodes for the 11-stage Dickson charge pump. Now, the fitted and measured results are relatively close.

The realised Fibonacci charge pump has higher values of the efficiency and output voltage than the Dickson charge pump. The Fibonacci charge pump is suitable for a higher value of the voltage gain and requires more transistors than the Dickson charge pump. But the number of used diodes and capacitors for the Fibonacci charge pump is lower than for the Dickson charge pump. The Fibonacci pump concept is especially attractive to the pumps realised by discrete components, as the voltage gain for an intermediate number of stages is high. On the other hand, this charge pump type is not so suitable for integration into ASICs, because its sensitivity for on-chip parasitics is higher than e.g. for the Dickson-based architectures.

The measured parameters verify a possibility of the realisation of the Dickson and the Fibonacci charge pump in its discrete form. In the next period, the issue of the clock drivers for DCP will be resolved. The driving capability will be increased by splitting capacitors into sections. Each section will be driven by a separate clock driver. The FCP will be then extended by an auxiliary current limiter for the inverter in each stage. Other types of transistors with a lower threshold voltage will be finally used.

## ACKNOWLEDGMENT

This work has been supported by the grant No. SGS17/183/OHK3/3T/13 of the CTU in Prague.

## REFERENCES

[1] Dickson, J.F. (1976). On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique. *IEEE Journal of Solid-State Circuits*, 11 (3), 374-378.

[2] Pan, F., Samaddar, T. (2006). *Charge Pump Circuit Design*. McGraw-Hill Education.

[3] Seeman, M.D., Sanders, S.R. (2008). Analysis and optimization of switched-capacitor DC–DC converters. *IEEE Transactions on Power Electronics*, 23 (2), 841-851.

[4] Ueno, F., Inoue, T., Oota, I., Harada, I. (1991). Emergency power supply for small computer systems. In *IEEE International Symposium on Circuits and Systems*, 11-14 June 1991. IEEE, 1065-1068.

[5] Tanzawa, T. (2016). Innovation of switched-capacitor voltage multiplier: Part 1: A brief history. *IEEE Solid-State Circuits Magazine*, 8 (1), 51-59.

[6] Allasasmeh, Y., Gregori, S. (2009). A performance comparison of dickson and fibonacci charge pumps. In *European Conference on Circuit Theory and Design*, 23-27 August 2009. IEEE, 599-602.

[7] Matousek, D., Hospodka, J., Subrt, O. (2016). Efficiency of innovative charge pump versus clock frequency and MOSFETs sizes. *Measurement Science Review*, 16 (5), 260-265.

[8] Mayergoyz, I., Lawson, W. (2012). *Basic Electric Circuit Theory, 2nd Edition.* Academic Press.

[9] Tumanski, S. (2006). *Principles of Electrical Measurement*. CRC Press.

Received February 20, 2017.
Accepted April 28, 2017.