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An Improved Linearization Circuit Used for Optical Rotary Encoders

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Optical rotary encoders generate nonlinear sine and cosine signals in response to a change of angular position that is being measured. Due to the nonlinear shape of encoder output signals, encoder sensitivity to very small changes of angular position is low, causing a poor measurement accuracy level. To improve the optical encoder sensitivity and to increase its accuracy, an improved linearization circuit based on pseudo-linear signal generation and its further linearization with the two-stage piecewise linear analog-to-digital converter is presented in this paper. The proposed linearization circuit is composed of a mixed-signal circuit, which generates analog pseudo-linear signal and determines the first four bits of the final digital result, and the two-stage piecewise linear analog-to-digital converter, which performs simultaneous linearization and digitalization of the pseudo-linear signal. As a result, the maximal value of the absolute measurement error equals to $3.77168 \cdot 10^{-5}$ [rad] (0.00216°) over the full measurement range of 2π [rad].

Keywords: Angular position measurement, linearization, analog-to-digital conversion, accuracy improvement.

1. INTRODUCTION

In this paper, attention is devoted to the linearization of optical rotary encoder output signals by using an improved linearization circuit, which, in general, can be applied to other types of sensors with sinusoidal output signals, i.e. with magnetic sensors, resolvers [1]-[5], and sensors based on the Hall effect [6]. The application of the proposed linearization circuit overcomes the disadvantages of processor demanding digital techniques, while at the same time represents a more flexible solution in comparison to analog linearization techniques [7]. In [1], [2], the angular position determination method based on the knowledge of the resolver excitation signal amplitude is proposed. In particular, this method is based on a comparison between amplitudes of the pseudo-linear signal and the resolver excitation signal, so the additional errors, caused by the fluctuation and drift of the excitation signal amplitude are introduced. In paper [3], in order to obtain a signal that is as close as possible to an ideal triangular signal, the linearization of a signal representing a difference between the absolute values of demodulated resolver output signals is performed. As a result, for determination of the angular position, simpler linear equations can be used. However, the application of rectifying circuits for the resolver linearization leads to the introduction of additional nonlinearities. All the above-mentioned disadvantages can be avoided by using the linearization technique proposed in this paper.

The linearization technique proposed in this paper includes two phases: 1. generation of a pseudo-linear signal and the first four bits of the final digital result; and 2. simultaneous linearization and digitalization of the pseudo-linear signal.

2. PROPOSED LINEARIZATION CIRCUIT

The proposed linearization circuit is composed of two circuits: 1. a special-purpose 4-bit mixed-signal circuit used for pre-processing of co-sinusoidal signals in order to generate the pseudo-linear signal and the first four bits of the final digital result; and 2. a two-stage piecewise linear A/D converter (TSPLADC) used for simultaneous linearization and digitalization of the pseudo-linear signal obtained at the mixed-signal circuit output. The TSPLADC is a general-purpose linearization circuit, i.e. by reprogramming its transfer function any sensor type can be linearized [8]-[15].

Fig.1. shows the block diagram of the mixed-signal circuit. By observing Fig.1., one can notice three building blocks of the circuit: an analog signals generating block, a block for the generation of the first four bits of the final digital result (D_{n-1}, D_{n-2}, D_{n-3} and D_{n-4}, where n stands for the overall resolution $n=4+N_1+N_2$, including resolutions N_1 and N_2 of the first and the second conversion stage of the TSPLADC, respectively), and a 16 to 1 analog multiplexer (AMUX), which is controlled by the four generated bits.

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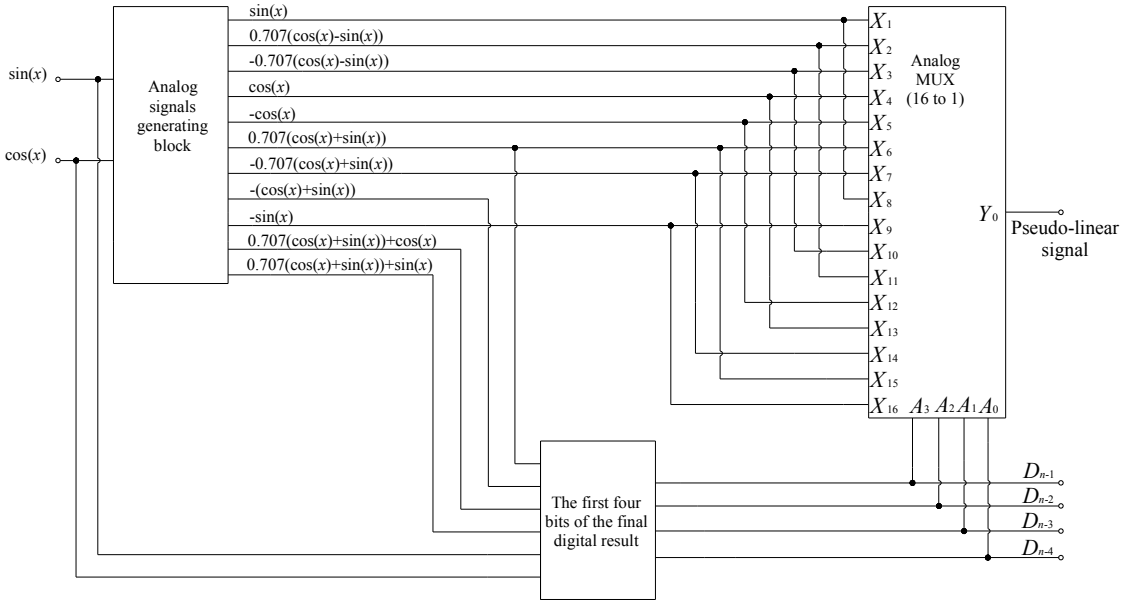

Fig.1. Block diagram of the 4-bit mixed-signal circuit used for the pseudo-linear signal generation.

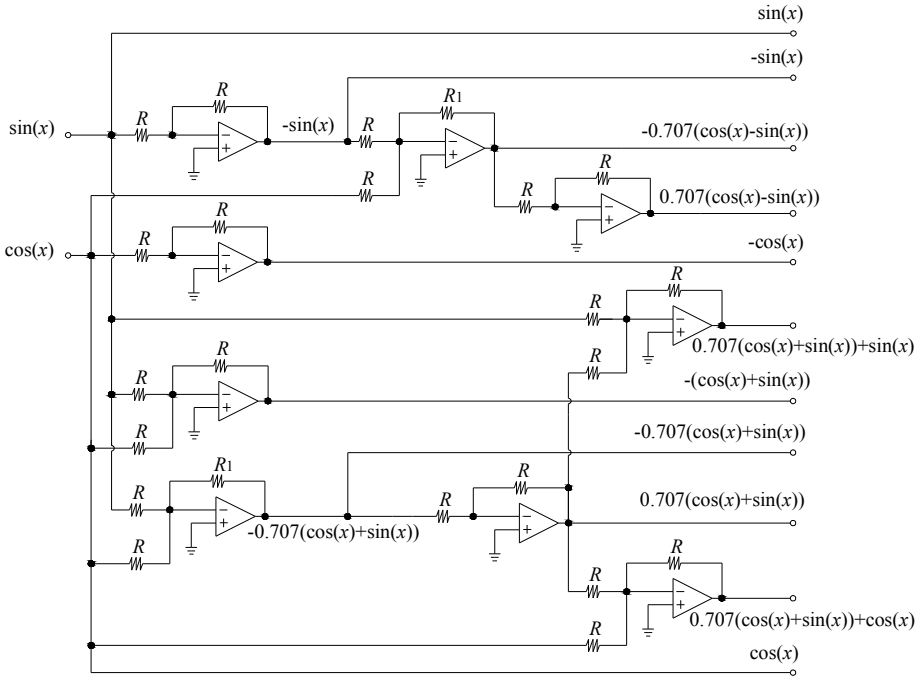

Fig.2. Analog signals generating block.

A detailed schematic of the analog signals generating block is shown in Fig.2. The circuit is comprised of operational amplifiers and required resistors R=1 kΩ and R_1=0.707 kΩ. The resistor R_1 represents, in fact, a serial connection between two resistors: 680 Ω and 27 Ω.

In order to clarify the reason why these analog signals are needed, in Fig.3. are shown their waveforms together with the pseudo-linear signal waveform (bolded line). These waveforms are obtained by simulating the proposed mixed-signal circuit in the LabVIEW software. Signals representing the sum of, or the difference between, sine and cosine signals multiplied by 0.707 (or $\sqrt{2}/2$) are obtained by phase shifting the sine and cosine signal for π/4 [rad], while the signals representing the sum of, or the difference between, sine and cosine signal multiplied by -0.707 (or-$\sqrt{2}/2$) are obtained by inverting the sine and cosine signal phase shifted for π/4 [rad]. Signals, which exhibit a higher level of linearity in certain segments (π/8 [rad] wide) in comparison to the original co-sinusoidal signals, are obtained in this manner. The pseudo-linear signal amplitude is equal to:

$\sin(\pi/8)\cdot A = 0.383\cdot A$ [V], where A [V] stands for the amplitude of co-sinusoidal signals.

The pseudo-linear signal represents a combination of the most linear fragments of eight analog signals shown in Fig.2. and Fig.3. These are the following signals:

$$S_1 = \sin(x), \tag{1}$$

$$S_2 = \cos\left(x+\frac{\pi}{4}\right) = \frac{\sqrt{2}}{2}\left(\cos(x)-\sin(x)\right), \tag{2}$$

$$S_3 = -\cos\left(x+\frac{\pi}{4}\right) = -\frac{\sqrt{2}}{2}\left(\cos(x)-\sin(x)\right), \tag{3}$$

$$S_4 = \cos(x), \tag{4}$$

$$S_5 = -\cos(x), \tag{5}$$

$$S_6 = \sin\left(x+\frac{\pi}{4}\right) = \frac{\sqrt{2}}{2}\left(\cos(x)+\sin(x)\right), \tag{6}$$

$$S_7 = -\sin\left(x+\frac{\pi}{4}\right) = -\frac{\sqrt{2}}{2}\left(\cos(x)+\sin(x)\right), \tag{7}$$

$$S_8 = -\sin(x). \tag{8}$$

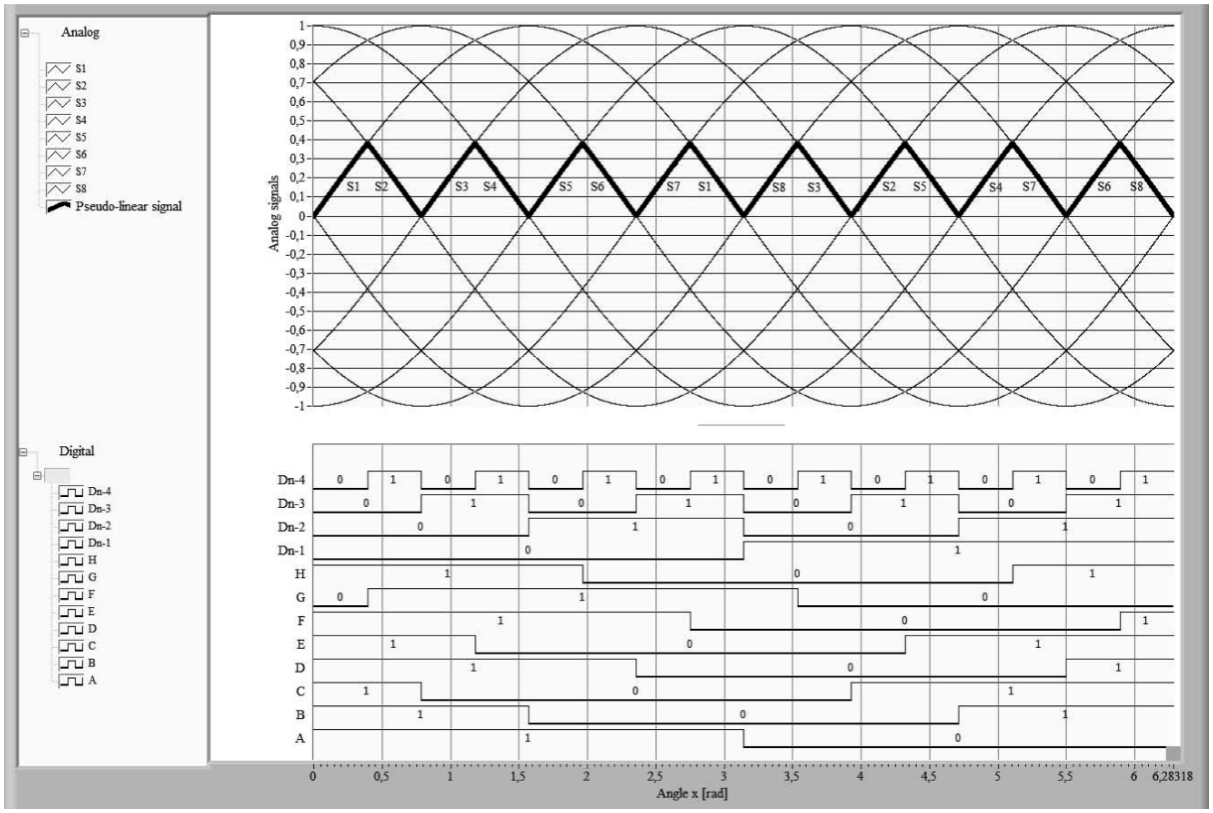

Fig.3. Analog and digital signals in different points of the mixed-signal circuit.

Each of these signals appears two times at the AMUX output, meaning that the pseudo-linear signal is composed of 16 fragments in the range from 0 to 2π [rad]. Which fragment is obtained at the AMUX output is determined by the bits D_{n-1}, D_{n-2}, D_{n-3} and D_{n-4}, generated by the circuit shown in Fig.4. Additionally, the circuit shown in Fig.2. generates three signals (S_6+S_4, S_6+S_1, $-(S_1+S_4)$) that are not used for pseudo-linear signal generation, but are essential for the determination of bits D_{n-1}, D_{n-2}, D_{n-3} and D_{n-4}.

Digital signals A, B, C, D, E, F, G and H (Fig.4.) represent the results of comparisons given in Table 1.

Table 1. Digital signals generated in order to obtain the first four bits of the final digital result.

Digital signal	Comparison
A	$\sin(x)>0$
B	$\cos(x)>0$
C	$\cos(x)>\sin(x)$
D	$\cos(x)+\sin(x)>0$
E	$0.707(\cos(x)+\sin(x))>\sin(x)$
F	$0.707(\cos(x)+\sin(x))+\sin(x)>0$
G	$0.707(\cos(x)+\sin(x))>\cos(x)$
H	$0.707(\cos(x)+\sin(x))+\cos(x)>0$

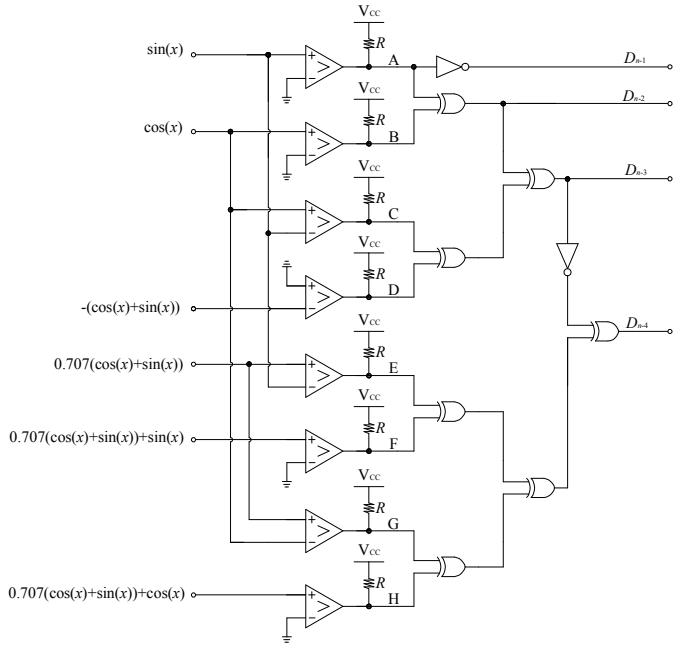

Fig.4. The block for the generation of the first four bits of the final digital result.

By conducting simple logical operations over digital signals (A…H), the bits $D_{n\text{-}1}$, $D_{n\text{-}2}$, $D_{n\text{-}3}$ and $D_{n\text{-}4}$ are generated:

$$D_{n-1} = \overline{A}, \tag{9}$$

$$D_{n-2} = A \,\mathrm{XOR}\, B, \tag{10}$$

$$D_{n-3} = \left(A \,\mathrm{XOR}\, B\right) \mathrm{XOR} \left(C \,\mathrm{XOR}\, D\right), \tag{11}$$

$$D_{n-4} = \left(\left(E \,\mathrm{XOR}\, F\right) \mathrm{XOR} \left(G \,\mathrm{XOR}\, H\right)\right) \mathrm{XOR}\, \overline{D}_{n-3}. \tag{12}$$

As it can be seen from Table 1., in order to generate digital signals (A…H) no additional reference voltage is used, as it is proposed in [1], [2], where it consequently led to the introduction of additional errors.

Since the pseudo-linear signal has the shape of sin(x) signal in each segment (see Fig.3.), it is sufficient to linearize sin(x) signal within one segment and have the information about that segment (bits $D_{n\text{-}1}$, $D_{n\text{-}2}$, $D_{n\text{-}3}$, $D_{n\text{-}4}$). As a result, linearization of the pseudo-linear signal with the TSPLADC is always performed within one segment. However, the slope of the pseudo-linear signal is negative in even segments, so in order to obtain a linear and monotonically rising transfer function, inversion of bits D_0-$D_{n\text{-}5}$ is necessary in even segments. The inversion is performed by bringing the bits D_0-$D_{n\text{-}5}$ to the inputs of XOR circuits together with the bit $D_{n\text{-}4}$ (see Fig.5.).

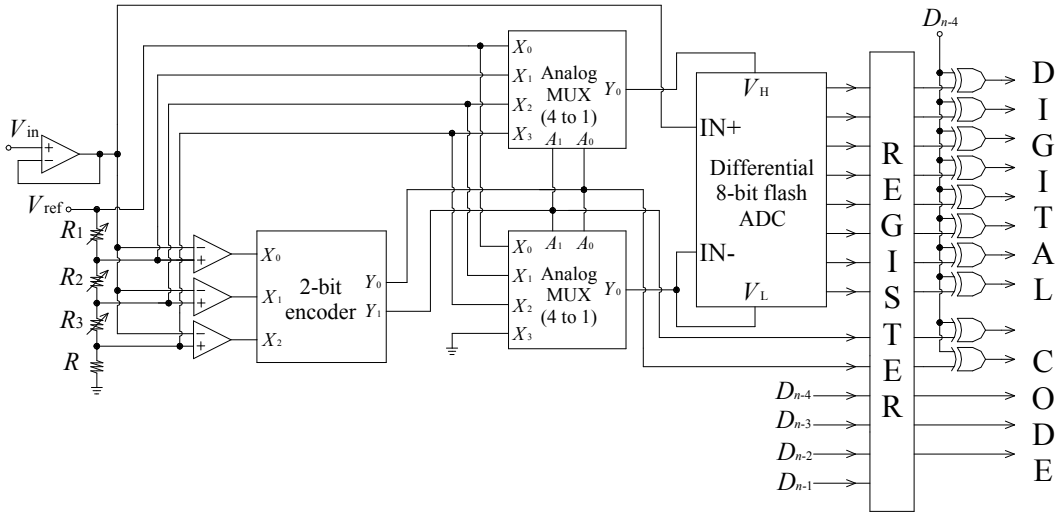

Fig.5. The two-stage piecewise linear analog-to-digital converter (TSPLADC).

The TSPLADC performs two conversion stages. The first conversion stage is performed by the piecewise linear flash A/D converter (ADC) having the input range non-uniformly divided into regions of unequal width in order to better approximate the function inverse to the dependence of the pseudo-linear voltage on the measured angle. In this manner, the non-linearity of pseudo-linear signal is compensated. The flash ADC employed in the second conversion stage is linear and it does not perform linearization. However, it reduces the quantization noise introduced in the signal during the first conversion stage, which in a smaller percentage reduces the overall measurement error. The input range of the second conversion stage is defined by the boundaries of the non-uniform region determined in the first conversion stage, and to which the current value of the measured angle belongs.

In the example shown in Fig.5., the first conversion stage is with the resolution of N_1=2 bits. For the realization of the 2-bit flash ADC a network of four resistors is needed in order to adjust the reference voltages of the comparators. Since the circuit proposed in this paper is intended just for the linearization of the optical rotary encoder, the reference voltages, i.e. so-called break voltages, are set only once by

using the variable resistors R_1, R_2 and R_3. The break voltages V_i, determined in the following manner:

$$V_i = \sin\left(i \cdot \frac{1}{2^{N_1}} \cdot \frac{\pi}{8}\right), \; i=1, 2,\ldots, 2^{N1}\text{-}1, \tag{13}$$

represent the boundaries of the non-uniform regions that compose the first stage flash ADC input range. Different solutions of the TSPLADC used for sensor linearization have been proposed during time, and among them are some that are considered as energy efficient [14], [15].

3. SIMULATION AND NUMERICAL RESULTS

The proposed 4-bit mixed-signal circuit is simulated using the Multisim software. Also, the overview of numerical results concerning the proposed circuit and their comparison with the corresponding parameters obtained using the previous version of the proposed circuit are given. The previous version of the linearization circuit is composed of the 3-bit mixed-signal circuit and the TSPLADC of the same design as the one described in this paper. In both cases the numerical results are generated using the LabVIEW software.

The simulation is an important indicator that the newly designed circuit is going to work as expected. Therefore, the simulation is a preceding step to the realization of a newly designed circuit which can prevent the loss of funds and time if there is an error in the circuit design. For the Multisim simulation of the proposed 4-bit mixed-signal circuit, commercially available components are used: LM224N operational amplifiers, LM239D comparators, 4030BT logical XOR circuits, 4049BD HEX inverting buffers, ADG406BN analog multiplexer, and adequate voltage supplies and resistors. Fig.6. shows simulation scope shoot of sine and cosine inputs and the AMUX output signal. The sine (yellow, CH1), cosine (blue, CH2), and pseudo-linear (green, CH4) signal from Fig.6. fully correspond to the expected theoretical results shown in Fig.3.

The simulation results obtained in Multisim can be closely considered as experimental due to the fact that the simulation is carried out using commercially available components. Therefore, it can be expected that the realization of the proposed 4-bit mixed-signal circuit, with the same components, will function in agreement with theory.

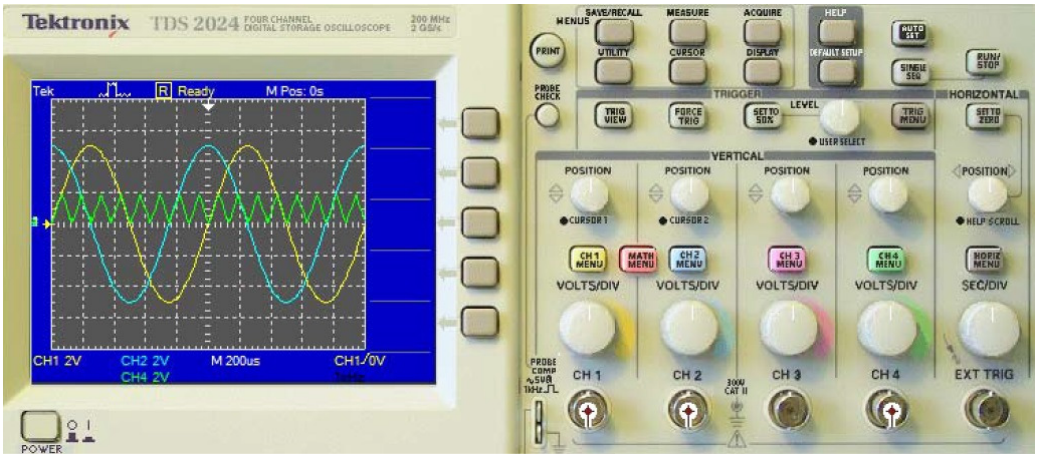

Fig.6. Scope shoot of sine (yellow, CH1) and cosine (blue, CH2) inputs, and the AMUX output signal (green, CH4) for the proposed 4-bit mixed-signal consisting of commercially available components.

The assessment of the performances and the comparison of the proposed linearization circuit to its previous version containing the 3-bit mixed-signal circuit [12], are performed based on the values of the following parameters: the maximal value of the absolute measurement error Δx [rad] and the value of nonlinearity δx [%], which are defined by the expressions (14) and (15), respectively:

$$\Delta x[\text{rad}] = \left| x_{\text{out}} - x_{\text{in}} \right|, \tag{14}$$

$$\delta x[\%] = \frac{\Delta x_{\max}[\text{rad}]}{2\pi[\text{rad}]} \cdot 100\%. \tag{15}$$

Two parameters are figuring in the expression (14): x_{in} [rad], which represents the actual, or the correct value of the measured angle x that is fed to the encoder input, and x_{out} [rad], which represents the output, i.e. the measured value of angle x after the linearization is finished. In the expression (15), $\Delta x_{\max}$ [rad] represents the maximal value of the absolute measurement error, while 2π [rad] denotes the full measurement range [16].

By using the LabVIEW software, two measurement system solutions were examined: one, with the proposed linearization circuit, and one with its previous version [12]. In the virtual instrument, which in addition to the mixed-signal circuit (3-bit or 4-bit), simulates the TSPLADC function, the parameter x_{in} is predefined, while the

parameter x_{out} is calculated. Thus, the virtual instrument determines the value of x_{out} as a function of: 1. x_{in} value; 2. the mixed-signal circuit resolution; 3. the pseudo-linear signal amplitude (which in case the 3-bit mixed-signal circuit is employed equals to $0.707 \cdot A$ [V], [12]); and 4. the resolutions of the first and the second conversion stage.

In Table 2. to Table 5., the maximal value of the absolute measurement error and the nonlinearity value, for different combinations of resolutions N_1 and N_2, are given. The resolutions denoted with N_1' and N_2' refer to the solution with the 3-bit mixed-signal circuit, while the resolutions denoted with N_1" and N_2" refer to the solution with the 4-bit mixed-signal circuit. The following cases were investigated:

Case 1 is illustrated in Table 2., in which the performances of both linearization circuits are given. Both solutions employ the TSPLADC of the same resolution in both conversion stages (N_1'=N_1", N_2'=N_2");

Case 2 is illustrated in Table 3. and represents a situation in which the first conversion stage of the TSPLADC does not perform the linearization, while the second conversion stage resolutions for both solutions are mutually equal (N_1'=N_1"=0, N_2'=N_2");

Case 3 is illustrated in Table 4. and represents a situation in which the first conversion stage of the TSPLADC does not perform the linearization, while the overall resolutions of both solutions are mutually equal (N_1'=N_1"=0, 3+N_2'=4+N_2", i.e. N_2'=1+N_2");

Case 4 is illustrated in Table 5. and represents a situation in which the overall resolutions of both linearization circuit solutions are mutually equal, whereby the first stage resolution N_1' is 1 bit higher than the resolution N_1" (N_1'=1+N_1", 3+N_1'+N_2'=4+N_1"+N_2").

These cases are analyzed in order to understand whether a greater reduction of the maximal absolute measurement error and nonlinearity is achieved by increasing the mixed-signal circuit resolution or by increasing the first conversion stage resolution, since both circuits perform linearization. Additionally, the aforementioned circuits' complexities increase disproportionately to the resolution.

Table 2. Case 1 (N_1'=N_1", N_2'=N_2").

3-bit mixed-signal circuit				4-bit mixed-signal circuit				Improvement ratio
N_1'	N_2'	Δx_{max}' [rad]	δx' [%]	N_1"	N_2"	Δx_{max}" [rad]	δx" [%]	Δx_{max}'/Δx_{max}", δx'/δx"
0	16	0.0331395	0.527432	0	16	0.0039538	0.0629266	8.381683
2	6	0.00849212	0.135156	2	6	0.00265563	0.0422656	3.19778
2	8	0.00506459	0.0806055	2	8	0.000998315	0.0158887	5.073138
2	10	0.00423256	0.0673633	2	10	0.000570334	0.00907715	7.421195
2	12	0.00402371	0.0640393	2	12	0.000464183	0.0073877	8.66837
2	14	0.00397232	0.0632214	2	14	0.000439342	0.00699234	9.041521
3	8	0.00162663	0.0258887	3	8	0.000388711	0.00618652	4.184677
3	10	0.00122258	0.019458	3	10	0.000183311	0.00291748	6.669431
3	12	0.0011233	0.0178778	3	12	0.000131922	0.00209961	8.51488
3	14	0.00109762	0.0174692	3	14	0.000119521	0.00190224	9.183491
4	8	0.000568493	0.00904785	4	8	0.000169658	0.0027002	3.350817
4	10	0.000349364	0.0055603	4	10	6.35068E-5	0.00101074	5.501206
4	12	0.000303134	0.00482452	4	12	3.77168E-5	0.000600281	8.037108

Table 3. Case 2 (N_1'=N_1"=0, N_2'=N_2").

3-bit mixed-signal circuit				4-bit mixed-signal circuit				Improvement ratio
N_1'	N_2'	Δx_{max}' [rad]	δx' [%]	N_1"	N_2"	Δx_{max}" [rad]	δx" [%]	Δx_{max}'/Δx_{max}", δx'/δx"
0	6	0.0513454	0.817188	0	6	0.0131063	0.208594	3.917612
0	8	0.0376697	0.599531	0	8	0.00615556	0.0979688	6.119622
0	10	0.0342421	0.54498	0	10	0.00449825	0.0715918	7.612316
0	12	0.0333929	0.531465	0	12	0.00408392	0.0649976	8.176678
0	14	0.0331943	0.528304	0	14	0.00397777	0.0633081	8.344952
0	16	0.0331395	0.527432	0	16	0.0039538	0.0629266	8.381683

Table 4. Case 3 ($N_1'=N_1''=0$, $3+N_2'=4+N_2''$, i.e. $N_2'=1+N_2''$).

3-bit mixed-signal circuit				4-bit mixed-signal circuit				Improvement ratio
N_1'	N_2'	$\Delta x_{max}'$ [rad]	$\delta x'$ [%]	N_1''	N_2''	$\Delta x_{max}''$ [rad]	$\delta x''$ [%]	$\Delta x_{max}'/\Delta x_{max}''$, $\delta x'/\delta x''$
0	7	0.0422544	0.6725	0	6	0.0131063	0.208594	3.223976
0	9	0.0354165	0.563672	0	8	0.00615556	0.0979688	5.753579
0	11	0.0336703	0.535879	0	10	0.00449825	0.0715918	7.4852
0	13	0.0332628	0.529395	0	12	0.00408392	0.0649976	8.144822
0	15	0.0331601	0.527759	0	14	0.00397777	0.0633081	8.336354
0	17	0.0331318	0.52731	0	16	0.0039538	0.0629266	8.379736

Table 5. Case 4 ($N_1'=1+N_1''$, $3+N_1'+N_2'=4+N_1''+N_2''$).

3-bit mixed-signal circuit				4-bit mixed-signal circuit				Improvement ratio
N_1'	N_2'	$\Delta x_{max}'$ [rad]	$\delta x'$ [%]	N_1''	N_2''	$\Delta x_{max}''$ [rad]	$\delta x''$ [%]	$\Delta x_{max}'/\Delta x_{max}''$, $\delta x'/\delta x''$
1	16	0.01296	0.206265	0	16	0.0039538	0.0629266	3.27786
3	6	0.00328395	0.0522656	2	6	0.00265563	0.0422656	1.236599
3	8	0.00162663	0.0258887	2	8	0.000998315	0.0158887	1.629375
3	10	0.00122258	0.019458	2	10	0.000570334	0.00907715	2.143621
3	12	0.0011233	0.0178778	2	12	0.000464183	0.0073877	2.419951
3	14	0.00109762	0.0174692	2	14	0.000439342	0.00699234	2.498327
4	8	0.000568493	0.00904785	3	8	0.000388711	0.00618652	1.462508
4	10	0.000349364	0.0055603	3	10	0.000183311	0.00291748	1.905854
4	12	0.000303134	0.00482452	3	12	0.000131922	0.00209961	2.297827
4	14	0.000289443	0.00460663	3	14	0.000119521	0.00190224	2.421692
5	8	0.000212456	0.00338135	4	8	0.000169658	0.0027002	1.25226
5	10	0.00010619	0.00169006	4	10	6.35068E-5	0.00101074	1.672104
5	12	8.05148E-5	0.00128143	4	12	3.77168E-5	0.000600281	2.13472

Case 1: By comparing measurement error and nonlinearity values given in Table 2., a significant improvement is observed in the case when the 4-bit mixed-signal circuit is employed. The improvement is defined as the ratio between $\Delta x_{max}'$ and $\Delta x_{max}''$, or between $\delta x'$ and $\delta x''$. The improvement ratio higher than 1 implies that the linearization circuit proposed in this paper shows better performances in comparison to the solution proposed in [12]. A difference between $\Delta x_{max}'$ and $\Delta x_{max}''$ is greater when the resolution of the TSPLADC is higher.

Case 2: In this case, resolutions N_1' and N_1'' are equal to 0 meaning that the linearization is not performed with the TSPLADC. The improvement ratio increases with the increase of the second stage resolution. This case is a sub-case of Case 1, which is singled out in order to observe the influence of the second stage resolution on the linearization circuit performances.

Case 3: In this case, the same as in Case 2, the linearization by the first conversion stage is not performed, i.e. $N_1'=N_1''=0$. However, in this case the resolution N_2' is 1 bit higher than N_2'', resulting in lower improvement ratios in comparison to Case 2. Although the overall resolutions for both solutions are the same, the solution employing the 4-bit mixed-signal circuit has better performances because the improvement ratio is higher than 1. This is the case when the influence of the mixed-signal circuit resolution on the linearization circuit performances is singled out.

Case 4: In this case, although the resolution N_1' is 1 bit higher than N_1'', better performances are achieved using the linearization circuit with the 4-bit mixed-signal circuit. From here, one can conclude that the main contribution to the nonlinearity reduction and accuracy improvement is achieved using the 4-bit mixed-signal circuit. In other words, higher resolution of the mixed-signal circuit has provided the greatest improvement in the optical rotary encoder accuracy. The previous statement justifies the need for a certain level of complexity increase of the mixed-signal circuit used for the pseudo-linear signal generation. However, the improvement ratio in this case has the lowest values due to the fact that the resolution N_1' is 1 bit higher than N_1''. Continuation of the resolution N_1' increase leads to the improvement of performances of the linearization circuit with the 3-bit mixed-signal circuit. However, high resolution of the first conversion stage makes the piecewise linear flash ADC complexity high, i.e. a large number of non-uniform break (reference) voltages needs to be calculated and adjusted using more components, such as variable resistors. In addition, each time the flash ADC resolution increases by 1 bit the number

of employed comparators doubles making their matching and proper biasing more difficult [17]. Also, the complexity and the power consumption of the ADC are increased. In other words, it is preferable to exploit the 4-bit mixed-signal circuit than to increase the resolution of the first stage flash ADC. When both linearization circuit solutions have the same overall resolution, the lower measurement error is achieved with a circuit having the mixed-signal circuit with higher resolution than the circuit having the first conversion stage with higher resolution (see Table 5.).

To realize all the benefits of the linearization circuit proposed in this paper it is important to compare it with other linearization solutions proposed in the literature. The paper [6] describes a converter that is using alternating pseudo-linear segments of output co-sinusoidal signals from a Hall effect sensor, together with a simple and effective linearization technique. The theoretical absolute error of this converter is 0.05° over the full 360° range. In paper [5], a robust amplitude to phase converter, developed for the determination of position using the sine and cosine output signals of a resolver, is described. The theoretical absolute error in this case equals to 0.0082° over the full 360° range. However, the maximal absolute error obtained by applying the linearization circuit proposed in this paper (4-bit mixed-signal circuit and TSPLADC with N_1=4 bits and N_2=12 bits), equals to 0.00216° ($3.77168 \cdot 10^{-5}$ [rad]) over the full 360° (2π [rad]) range. As one can notice, in comparison to the result obtained in [6] the maximal absolute error obtained in this paper is more than twenty times lower, while in comparison to the result given in [5] it is four times lower. In addition, in papers [5] and [6] the information about the angle is obtained in analog format, while in this paper the angular position is converted into a digital format, which is very important since the majority of newly developed measurement systems are digital. Also, the linearization and digitalization are performed simultaneously by the same circuit, reducing in this manner the signal processing time, circuit complexity and its production costs and power consumption.

4. CONCLUSIONS

In this paper an improved solution of the optical rotary encoder linearization circuit is proposed. The proposed circuit is composed of the 4-bit mixed-signal circuit and the two-stage piecewise linear A/D converter. The advantages of the proposed linearization circuit are highlighted through a comparison with its previous version that is using the 3-bit mixed-signal circuit for the generation of pseudo-linear signal. Higher resolution in the mixed-signal circuit allows extraction of more linear fragments from co-sinusoidal signals, so that the pseudo-linear signal, which is further linearized in the two-stage piecewise linear A/D converter, has a better linearity from the start. The lower values of the maximal absolute error and of the nonlinearity, obtained after the application of the proposed linearization circuit, represent a significant improvement linked to the mixed-signal circuit resolution increase. The analysis of numerical results has shown that a greater impact on the absolute measurement error reduction has the mixed-signal circuit resolution increase for one bit than the resolution increase of the first conversion stage, which is also performing the linearization. In other words, the linearization circuit with the 4-bit mixed-signal circuit achieves better results in comparison to the linearization circuit containing the 3-bit mixed-signal circuit and the first conversion stage with one bit higher resolution. In both cases the overall resolutions are the same. Therefore, it is more preferred to increase the complexity of the mixed-signal circuit instead of the complexity of the first conversion stage of the two-stage piecewise linear A/D converter.

The value of the maximal absolute measurement error, after the linearization is performed using the proposed circuit, equals to $3.77168 \cdot 10^{-5}$ [rad] (0.00216°) over the full 2π [rad] (360°) range, which is two times lower in comparison to the corresponding parameter related to the linearization circuit of the same overall resolution that is employing the 3-bit mixed-signal circuit. Also, the solution proposed in this paper provides lower absolute measurement error in comparison to the analog linearization schemes given in the literature, which usually require an additional ADC for the applications in digital measurement systems.

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