MEASUREMENT SCIENCE REVIEW, **19**, (2019), No. 3, 86-92

sciendo

ISSN 1335-8871

MEASUREMENT SCIENCE REVIEW

Journal homepage: https://content.sciendo.com

Digital Signal Processing Algorithm for Measurement of Settling Time of High-Resolution High-Speed DACs

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The paper presents the developed complex Digital Signal Processing algorithm for the reduction of white and 1/*f* noise and processing of the measurement signals of the Settling Time Measurement of the Digital-to-Analog Converters. The results show that the proposed DSP algorithm ensures 100-fold suppression of the white noise and 1/f noise. It was shown that it is possible to measure settling times of high-speed DACs (up to 16-17 Bits) with readout levels of ± 0.5 LSB while measurement errors do no exceed ± 1.4 ns.

Keywords: Digital filters, active noise reduction, Discrete Fourier transforms, sampling method, time measurement, computerized instrumentation.

1. INTRODUCTION

Precise measurements of parameters of electric signal waveforms are often required in modern applications of electronic measurements. Digital signal processing methods are often used for these purposes [1]-[4]. The main source of errors during such measurements is the noise generated in the circuitry like amplifiers, converters, bias circuits, etc. of a measured signal and the reduction of noise is an important topic [5]-[7]. Wide use of high-speed amplifiers, digital-to-analog (DAC) and analog-to-digital (ADC) converters and other high-speed circuitry defines that the parameters of such circuits need to be precisely measured. Since most of the analog signals are converted to digital form and processed using digital signal processing methods, nowadays it is often necessary to convert the digital signal back to analog form retaining the speed and accuracy of the resulting signal. Therefore, precise high-speed DACs are used.

There are DACs with up to 32 bits precision available on the market and relatively high-speed 16-bit DACs with settling times of ≤ 20 ns.

Settling time of the output signal is one of the most important parameters characterizing speed of high-speed DACs. The settling time is measured within the limits of ± 0.5 least significant bit (LSB). Having the full magnitude of DAC output signal 1 V, the ± 0.5 LSB levels equal to ± 7.63 μV. It is obvious that the measurements of settling time parameters are required and are not simple [8]-[10].

There is a measurement technique based on sampling converters for 18-bit DACs with settling times ≥30 ns [10]-[12]. Specialized sampling converters are used in order to prevent overloading of wideband oscilloscope inputs. One of the main disadvantages of such method is that settling times are measured on the screen of the oscilloscope and therefore it is not fast and requires a highly skilled operator. The method proposed is not suitable for measurement of DACs with settling times faster than 30 ns.

Automated settling time measurement testers for 8-10-bit high-speed DACs have been proposed previously [13]-[14]. Specialized compensating sampling converters as well as backward conversion of time base, normalization of the magnitude of the measurement signal of Device Under Test (DUT) and digital measurement of settling time have been implemented [13]-[17].

Measurement of a settling time of DACs with higher bit count was not possible using such testers because the internal noise of the sampling converters was too high and thus, reducing the noise by circuitry improvement is not feasible.

Therefore, conversion of the DUT measurement signal to the digital form after the time conversion in sampling converters, followed by amplification and averaging of several measurement signal instances was proposed [14]. It was shown that the proposed method reduces the level of internal noise 6-fold and the digital processing of the signal has allowed to measure settling times of 12-13-bit high-speed DACs.

DOI: 10.2478/msr-2019-0014

Nevertheless, for the measurement of settling times of DAC's with higher bit count a better method should be developed because the resulting DUT measurement signal after averaging still contains a certain amount of noise components which prevents measurement of a settling time with stricter measurement limits (within ± 0.5 LSB).

Previous works [14], [16] have shown that it is possible to partially distinguish the spectrum of the DUT measurement signal and noise components by using a number of measurement signal instances and forming a pseudo-periodic measurement signal sequence. This sequence is filtered using a brick-wall comb filter in the frequency domain. Such method allows effective reduction of the noise components up to 10 times while the measurement signal is not affected and allows settling time measurement for 13-14-bit high-speed DACs within ± 0.5 LSB [16].

For the measurement of settling times of high-speed 16-bit DACs with settling times of ≤ 20 ns it is necessary to reduce the residual noise components more effectively.

A complex algorithm has been developed and it has been shown that the noise is reduced 100-fold compared to the unprocessed measurement signal [16]. The algorithm for digital measurement of the settling time has been developed and initial investigations of the method have been presented in [17]. It is proposed to improve the efficiency of the digital processing algorithm by introducing the averaging of the spectral components of different realizations of the measurement signal instead of the averaging of the resulting measurement signals in the time domain. Results of further investigations of the repeatability of the settling time measurements using the proposed method when the measurement signal (output signal of DAC after sampling converter and ADC) of the 16-18-bit high-speed DACs is influenced by the white noise and 1/f noise (internal noise of the sampling converters and ADC) are presented in this paper.

2. INVESTIGATION OF COMPLEX ALGORITHM OF DIGITAL SIGNAL PROCESSING

The algorithm has been investigated using the LabView® model. A number of DUT measurement signal instances have been produced using a model of an ideal measurement signal after a reverse time base conversion and a model of white and/or 1/*f* noise [16].

$$u(t) = U_S + a_s e^{-b_s (t_G - t)} \sin[c_s (t_G - t) + d_s], \qquad (1)$$

here U_S – square DUT pulse, t_G – duration of the flat part of the DAC output pulse, a_s, b_s, c_s, d_s – approximation parameters of the output signal.

A series of generated DUT measurement signal instances is formed into a single pseudo-periodic sequence S_{INi} represented as a numeric array.

This array is sent to the Discrete Fourier Transformation (DFT) LabView $F_i[]$ module (Fig.1.). As the instances of a measurement signal form a pseudo-periodic sequence, the spectrum of the DUT measurement signal is approaching the discrete spectrum by increasing the number of signal periods. Having a higher number of instances of the signal, the side harmonics around the main harmonics mf_0 become relatively small and can be neglected.

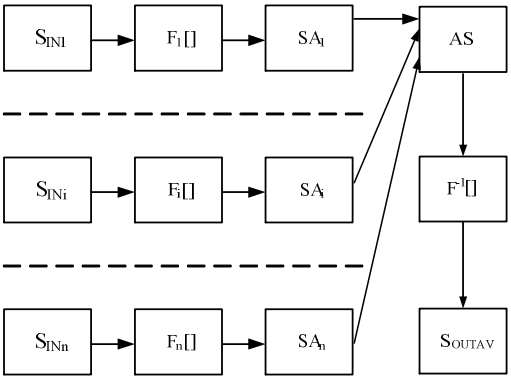

Fig.1. Structural diagram of a complex signal processing algorithm. S_{INi} – *i*-th input signal with noise; $F_i[]$ – *i*-th DFT module, SAi – *i*-th spectrum filtering module, AS – module of averaging of spectrum components, $F^{-1}{}_i[]$ –module of inverse DFT, S_{OUTAV} – output of a filtered signal.

The spectrum of the noise components is continuous as the noise components are nearly non-repeating over the instances of the measurement signal. This separation of spectrums allowed the development of a digital brick-wall comb filter in the frequency domain [14]:

$$H(f) = \begin{cases} 1, & \text{when } f = mf_0 \\ 0, & \text{elsewhere,} \end{cases} \qquad (2)$$

here f_0 – frequency of the main harmonic of DUT measurement signal, m = 1, 2, 3, ...

The output of the filter is an array of complex numbers of the filtered spectrum of the signal. Analysis of the effectiveness of the filter has shown that the spectral components of the noise with the frequency $f_n \neq mf_0$ are completely blocked and the spectral components $f_{nmf0} = mf_0$ of the noise are passing the filter unaffected. Therefore, these residual noise components are periodic and contain the same frequency components as the DUT measurement signal.

Previous research has shown that the effectiveness of this filter [14], [16] is not sufficient for the measurement of the settling times of 14-bit high-speed DACs. Further investigations have shown that magnitudes of the noise spectral components vary between the different instances of the pseudo-periodic measurement signal.

A complex signal processing algorithm has been developed to increase the effectiveness of the noise filtering. A number n_r of instances of a filtered (by using DFT modules $F_i[]$ and brick-wall comb filters SA_i) pseudo-periodic signal with noise components are sent to the module of averaging of Spectrum components (AS). Average values of a corresponding harmonics of the spectrums of the instances are calculated:

$$S_{iav} = \sum_{i=1}^{n_r} S_i \Big/ n_r \qquad (3)$$

The resulting array of a complex spectrum harmonics is sent to the module of an inverse Discrete Fourier Transformation F^{-1}[].

The resulting filtered instance of the DUT measurement signal is saved to the module S_{OUTAV} and used for the settling time measurement.

Further, the digital array of the white noise with standard deviation of $\sigma = 10$ mV has been added to the digital array of an ideal measurement signal. Number of pseudo-periodic sequences (up to 100 sequences) of n_i = 10, 20, 50, 80, 100 repetitions has been generated and processed by a complex algorithm.

The results (Fig.2.) show that 85-100 periods of the DUT measurement signal and 100 realizations of pseudo-periodic sequences are sufficient for averaging, while the white noise component is reduced by 90-100 times.

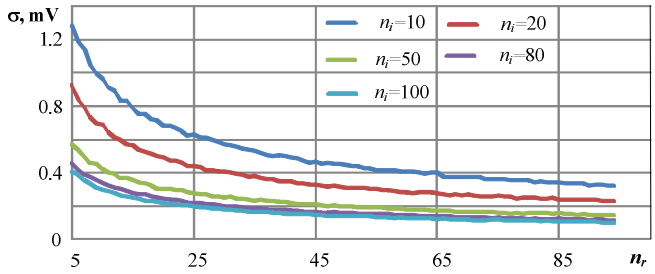

Fig.2. Noise level on the output of the processing algorithm on the number of realizations of the pseudo-periodic sequence (n_r) and different number of measurement signal realizations forming a pseudo-periodic sequence (n_i), standard deviation of the input signal noise set to 10 mV.

Similarly, the standard 1/*f* noise signal was generated by a LabView function. The standard deviation of the noise has been set to $\sigma_{IN} = 10$ mV and the cutoff frequency set to $F_{max} = 1.8$ kHz. The reduction of the 1/*f* noise component has been similar to the reduction of white noise (90-100 times).

With the 1/*f* noise cutoff frequency set to $F_{max} = 80$ Hz all the components of the noise have been removed by the processing algorithm.

Comparison of the ideal input signal (DUT measurement signal) and the output signal after the digital processing has shown that the signal form is not distorted or affected by the algorithm implementing the digital brick-wall comb filter and averaging functions. It has been established that there is a possibility to improve the processing results by selecting higher repetition frequency f_0 of the DUT measurement signal realizations while the sampling converters are developed so that the 1/*f* noise components with cutoff frequency $F_{max} \leq f_0$, where f_0 is the first harmonic of the generated DUT measurement signal pseudo-periodic sequence.

3. INVESTIGATION OF SETTLING TIME MEASUREMENT OF HIGH-SPEED DAC

In order to investigate the effectiveness of the developed noise reduction algorithm, the algorithm for evaluation of measurement errors has been developed.

The main measurement errors are coming from the definition of the measurement start moment, since the steepness of the DUT signal around the readout levels is typically not high. Small variations in detecting the exact moment of DUT signal becoming higher (or lower) than the readout levels lead to high measurement errors when the sampling converter and readout levels are set to ± 0.5 LSB. The resulting digital array of the filtered measurement signal is stored and used for the settling time measurement. The magnitude of the settled signal is measured and if it differs from the expected value the correction coefficient is calculated and all the values of the samples of the signal are multiplied by it.

Further, samples from the corrected signal are compared to the settling time measurement readout levels (± 0.5 LSB). The sample n_d which exceeds the readout level (is higher than the upper limit + 0.5 LSB or lower than the lower limit – 0.5 LSB) is the sample which starts the settling time measurement.

The sample of settling time measurement start n_t of the ideal measurement signal (with no noise added) is obtained the same way.

Therefore, the error of the settling time measurement start sample is:

$$\Delta t = (n_d - n_t)t_d \,, \tag{4}$$

where n_t – sample of the settling time measurement start of the ideal measurement signal, t_d – time interval between two samples of the DUT measurement signal, ns.

The time interval between two samples of the measurement signal of the real settling time tester is [14]:

$$t_d = \frac{1}{f_{ADC} q} \,, \tag{5}$$

where f_{ADC} – clock frequency of the ADC used in tester; q – time base transformation factor of the real sampling converter.

Different types and models of DACs lead to different processes of settling of the output signal, meaning different final voltage, rise and fall times, and the ringing (glitch) process itself. The type of the ringing of DUT output signal itself has a significant influence on the settling time measurement errors.

In order to investigate the effectiveness of the digital filtering on the measurement of settling time for different DAC signals, the ringing decrement of the DUT signal model has been set to be in agreement with parameters of fast DACs: Magnitude of a signal U_S = 1 V, t_G = 10 ms; frequency of the settling oscillations 20 kHz ($c_s = 1.25 \cdot 10^4$), and ringing decrement b_s = 45, 70, and 140 (corresponding to n_s = 6, 3 and 1 periods of settling oscillations).

Magnitude of the standard deviation of the white and 1/*f* noise has been changed during the investigations in order to obtain a ratio of noise level to the readout levels that is acceptable for settling time measurements.

Investigations have been performed by changing the ratio of the standard deviation of the noise to the ± 0.5 LSB

readout levels. The ratio shows the level of the internal noise of the sampling converter which is acceptable for DAC settling time measurement and the level of the measurement errors.

Different settling time readout levels corresponding to ± 0.5 LSB of 16-18-bit DAC have been set during the investigations. Dependencies of settling time measurement errors for 16-bit DAC with U_{l16} = ± 7.6 μV readout levels, 17 bit – U_{l17} = ± 3.8 μV, and 18 bit – U_{l18} = ± 1.9 μV on noise standard deviation ratio to readout levels are provided in Fig.3.

In Fig.3.a) it can be seen that for the 16 bit DAC with readout levels of U_{l16} ± 7.6 μV the standard deviation of the noise can exceed the readout levels 8-fold and the maximum measurement error of the settling time measurement shall not exceed $\delta t_s \leq$ (+0.8; –0.2) ns. It implies that a sampling converter with internal noise level that exceeds readout levels 8-fold can be used for settling time measurement of 6-bit high-speed DACs.

The measured magnitude of internal noise of the sampling converters developed by the authors, previously [13], was – 40–100 μV. The standard deviation was σ_n= 13–35 μV. Therefore, the ratio noise/readout level when σ_n =35 μV, is σ_n/U_{l16} = 3.5. According to Fig.3.a) it can be seen that using such sampling converters and the developed complex signal processing algorithm, the measurement errors shall be in the range of (+0.6; –0.2) ns for all measured DUT signals.

Modern high-speed 16-bit DACs available on the market have a settling time parameter of ≤ 20 ns. In this case relative settling time measurement errors caused by the noise components shall be in the range of (+3; –1) % and will not exceed requirements for such measurements.

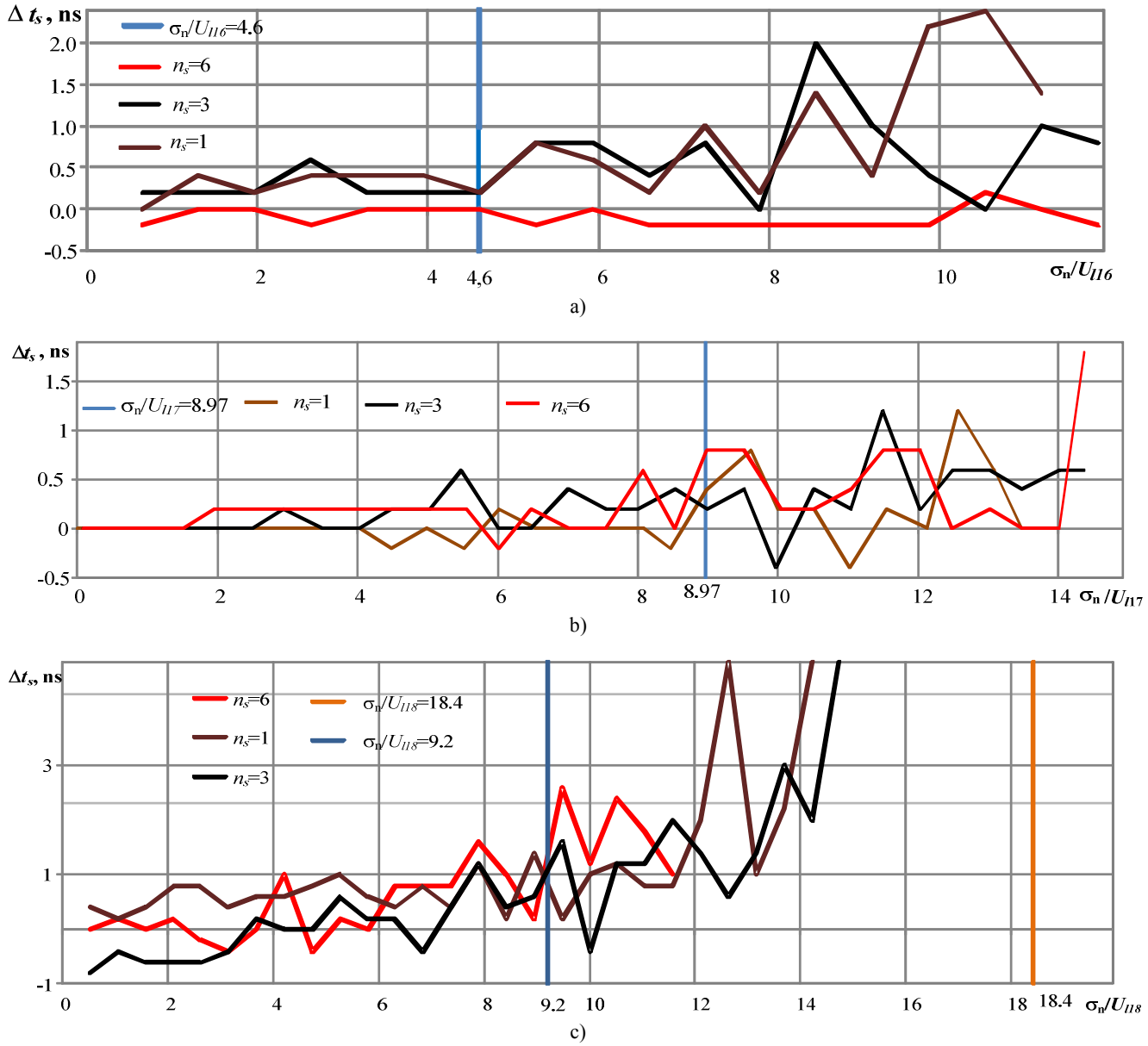

Fig.3. Dependency of the settling time measurement absolute error on the noise standard deviation ratio to the readout levels.
a) 16 bit DAC, 0.5 LSB readout levels U_l = ± 7.6 μV; b) white noise, 17 bit DAC, 0.5 LSB readout levels U_l = ± 3.6 μV; c) 18 bit DAC; 0.5 LSB readout levels U_l = ± 1.9 μV; numbers of DUT signal settling oscillations – n_s = 6; 3; 1.

Fig.3.b) shows that for the 17-bit DAC with readout levels set at $U_{l17} \pm 3.8$ µV the ratio noise/readout level can be up to $\sigma_n/U_{l17} = 10$ and the maximum settling time measurement error shall not exceed (+0.8; –0.3) ns ($n_s = 6$). The error shall not exceed +0.6 ns when $n_s = 3$ and shall not exceed +(0.5; –0.2) ns when $n_s = 1$. Therefore, the measurement of the settling time of the 17-bit DACs is possible using the developed signal processing method.

Fig.3.c) shows that for the 18 bit high-speed DAC the readout levels are set to $U_{l18} = \pm 1.9$ µV, the ratio noise/readout level can be up to $\sigma_n/U_{l18} = 10$ and the maximum settling time measurement error shall not exceed (+2.6; –0.4) ns in case $n_s = 6$; error shall not exceed (+1.2; –0.8) ns when $n_s = 3$, and shall not exceed +1.4 ns when $n_s = 1$.

Fig.3.c) shows that the settling time of 18-bit high-speed DACs cannot be measured using the developed signal processing algorithm if sampling converters with the internal noise standard deviation of $\sigma_n = 35$ µV are used. The results are provided in Fig.4. It can be seen that by setting the maximum cutoff frequency of $F_{ct} = 1.5$ kHz and the magnitude of 35 µV (the magnitude ratio of the $1/f$ noise to the readout levels is $\sigma_n \leq 9U_l$), the maximum settling time measurement error is not exceeding (+1.5; –0.5) ns.

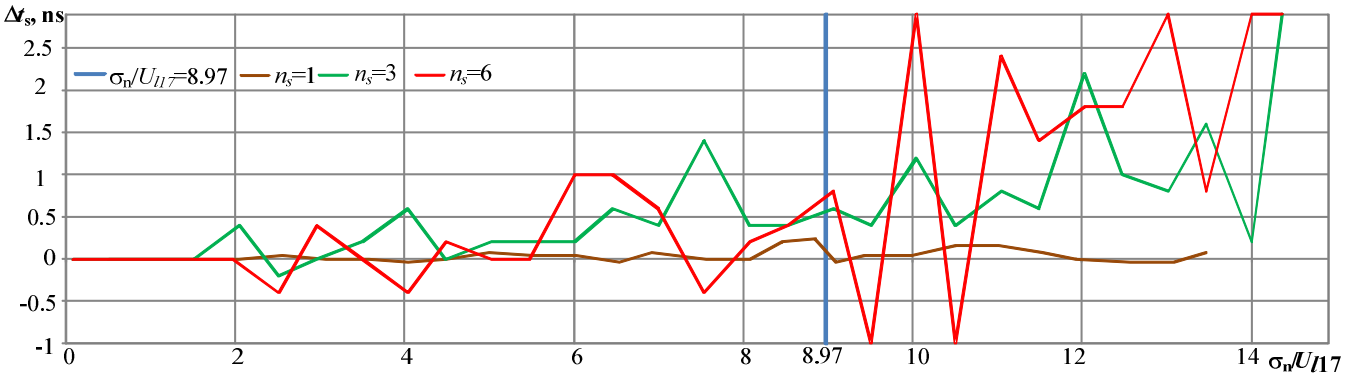

Fig.4. 17 bit DAC, dependency of the settling time measurement absolute error on the $1/f$ noise standard deviation ratio to the 0.5 LSB readout level ($U_l = \pm 3.6$ µV, and F_{ct}=1.5 kHz).

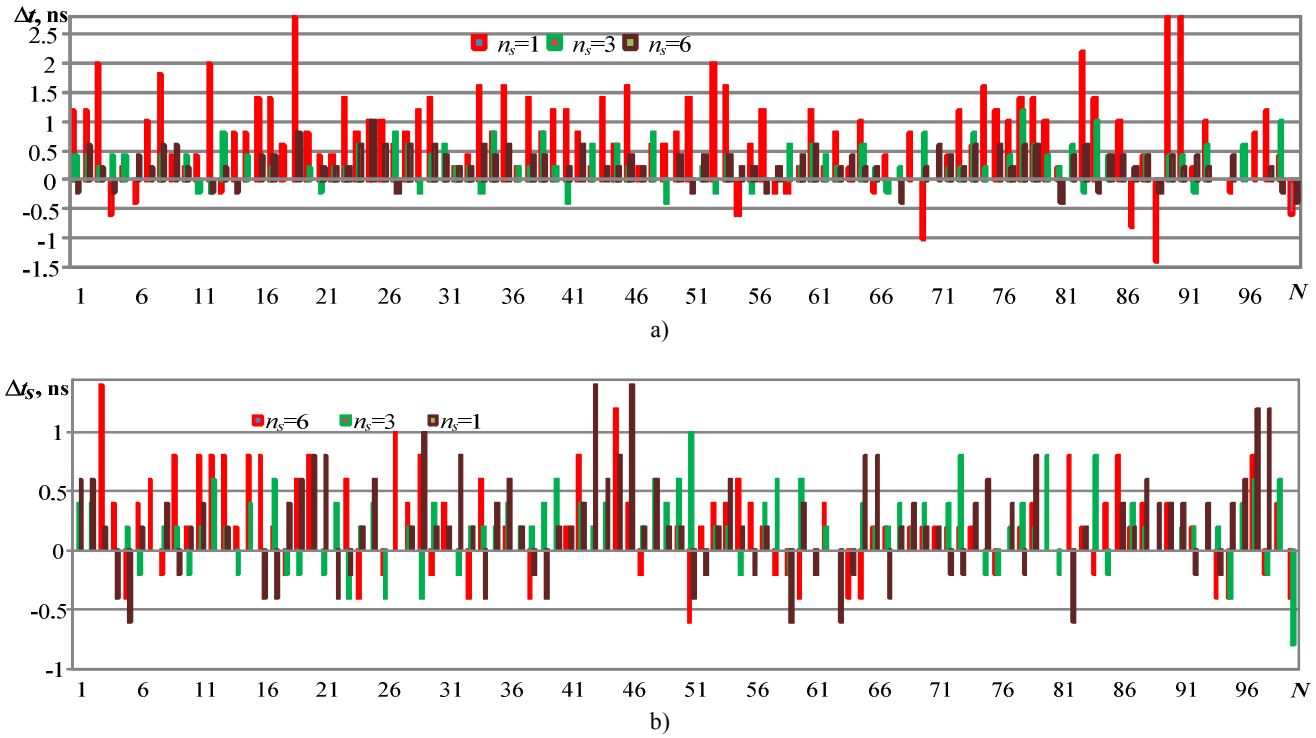

Fig.5. 17-bit DAC measurement repeatability, a) white noise with standard deviation $\sigma_n = 35$ µV; b) $1/f$ noise with magnitude $\sigma_n = 35$ µV and F_{ct}=2.2 kHz.

The investigation of the repeatability of the settling time measurement results with the developed signal processing algorithm has been also performed. Measurements have been conducted 100 times with different DUT measurement signal realizations. The investigation results are provided in Fig.5. It can be seen that the influence of the noise of the type $1/f$ with the cutoff frequency $F_{ct} \leq 1.5$ kHz on the stability of the measurement results is higher than the influence of the white noise. In case the cutoff frequency of the $1/f$ noise is set to $F_{ct} \leq 80$ Hz, the results are stable.

It has been established during the investigations that for some samples of DACs (earlier generations) with settling processes consisting of oscillations with more periods, there are situations when the measurement errors may increase at certain values of n_s. This effect is related to the situation when the magnitude of the n-th oscillation becomes relatively close to the readout level and even small amount of residual noise components may erroneously exceed readout levels. Therefore, further investigations on how to improve the digital processing algorithm will be performed.

Investigations have shown that one measurement of the settling time takes less than 3 seconds when standard PC (with Intel i5 CPU) is used. Such length of the measurement is acceptable for such applications.

4. CONCLUSION

1. It has been established that the DUT measurement signal after processing in the developed comb filter is fully periodic including its noise components and therefore it is not possible to further reduce the noise by averaging between periods of the same DUT sequence. Algorithm for filtering n_i pseudo-periodic sequences, each containing n_r periods of the DUT signals and then taking one period from each of the resulting filtered sequences and performing averaging, is proposed and investigated. It is established that implementation of all means of digital signal processing, including the comb filter and the averaging algorithm, reduces both white and $1/f$ noise level up to 100 times. LabView® virtual instrument implementing all of the represented means of digital signal processing and settling time measurement has been developed and investigated.
2. It has been shown that by setting the level of noise of a real sampling converter the proposed DSP algorithm and the settling time measurement algorithm is capable of measuring the settling time of the high-speed DACs up to 17 bit resolution with measurement errors not exceeding ± (+0.6; –0.2) ns with white noise applied, ± (+1.4; –0.2) ns for $1/f$ noise (≤ ± 3 % for white noise and ± 7 % $1/f$ noise when 20 ns DAC settling time is measured).
3. The complex DSP algorithm proposed is applicable for processing of other repeating measurement signals. By using this algorithm, it is possible to reduce the level of $1/f$ and white noise by 100 times without distortion of the measurement signal itself.
4. Out of 100 measurements with the noise standard deviation set to be 10 times higher than the readout levels (0.5 LSB), only 3 measurements have > + 3 ns errors. Therefore, additional measurements are required to improve the DUT signal processing algorithm, which may reduce errors and ensure settling time measurement for 18 bit and higher resolution DACs.
5. The proposed complex signal processing algorithm can be used for processing of various repeating measurement signals. It is possible to reduce noise levels of $1/f$ and white noise 100-fold without affecting the measurement signal itself.

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Received January 23, 2019
Accepted May 30, 2019