Uncertainty of the Dynamic DAC Testing by DC Voltage with Superimposed Dithering Signal

L. Michaeli, J. Šaliga, M. Sekerák, J. Lipták

Department of Electronics and Telecommunications,
Technical University of Košice, Letná 9, 041 20 Košice, Slovak Republic
Email: linus.michaeli@tuke.sk

Abstract. *The DAC testing method studied by authors is based on the comparison of a time-varying sawtooth signal generated by the DAC under test with a reference signal by a fast comparator. The reference signal is the superposition of DC voltage measured by a precise DC voltmeter and slow dithering voltage with known amplitude. The comparator detects the sequence of DAC control codes which determines the DAC nonlinearities. The paper provides analysis of the proposed method uncertainty. As results the requirement on the dithering voltage and DC precision will be estimated.*

Keywords: Digital to Analog Converter, DAC Dynamic Test, Dithering

1. Introduction

The appropriate use of such DACs requires a simple and reliable test procedure realizable in laboratories equipped with general purpose instruments. The common practical implementation of some of these test procedures is limited by requirements on instrumental equipment of laboratories performing standardized DAC testing [1]. Some of them require expensive high performance spectrum analyzers with high dynamic range and/or high quality notch filters. The authors proposed a dynamic DAC testing procedure in [2] based on the conversion of the DAC output level into record of the of input control codes of DAC under test in the fast memory. The registration instants are determined by the fast comparators.

2. Principle of the Proposed Method

A block diagram describing the proposed test method is shown in Fig. 1. The voltage comparator CMP compares the dynamic output voltage of the DAC under test (DAC UT) with the testing voltage $V_{SUM}= V_{DC}+ V_{DITH}$ created as a sum of reference DC voltage V_{DC} and a small superimposed dithering voltage V_{DITH}. Dithering voltage generated by the dithering DAC (D-DAC) with the known amplitude $W_{D\text{-}DAC}$ is attenuated by resistor divider $a=R_2/(R_1+R_2)$. Attenuation of D-DAC output suppresses the distortion of the dithering voltage V_{DITH}: [2]. The reference DC voltage is measured by a precise DC voltmeter with a long integration constant (Agilent 3458A), which ensures the averaging of the testing voltage and suppresses influence of the dithering voltage on DC measurement.

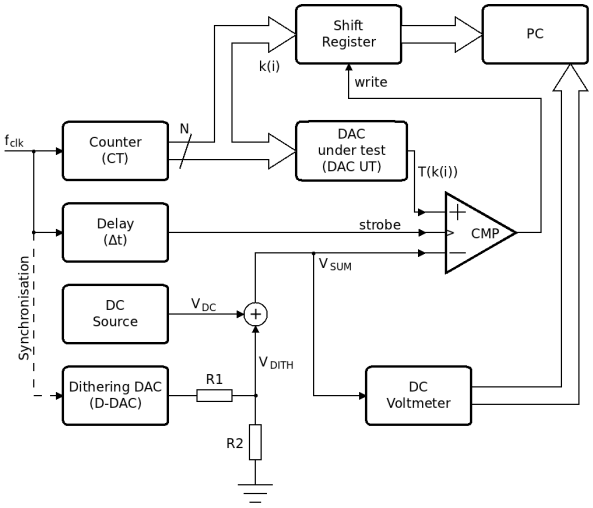
The difference ΔV(k) between the real transition code level T(k) and the known reference voltage VDC is proportional to the average number of the code words k(i) in the acquired record as it is shown in Fig. 1.b. The recorded code words k(i) are replaced by new values $p_k(i)$ equal to +1 or -1 as follows:

$$p_k(i)=\begin{cases} 1 & \text{if } k(i)\le k \\ -1 & \text{if } k(i)>k \end{cases} \qquad (1)$$

Then the voltage difference $\Delta V(k)$ between the tested transient code level $T(k)$ and the analog voltage V_{DC} measured by the precise voltmeter for the known amplitude W of the dithering

signal can be estimated as: .The known V_{DC} voltage measured with high precision allows to determine the transition code level $T(k)$ at the DAC UT for code k can be:

$$T(k) = V_{DC} + \Delta V(k) \cong V_{DC} + W \cdot \frac{1}{M} \sum_{i=1}^{M} p_k(i) \tag{2}$$



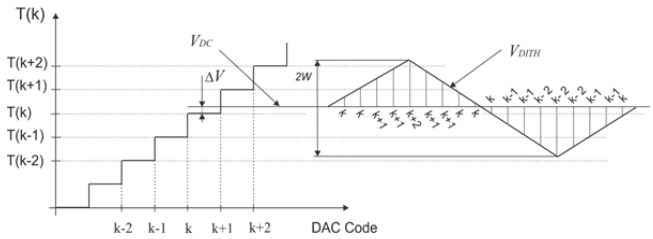


Fig. 1. a.) Block diagram of the proposed test method setup b.) and registration of input codes during one dithering period.

Where M is record length and W is peak-peak value of dithering voltage. The tested transition code levels $T(k)$ allow to estimate differential $DNL(k)$ according formulas [1].

$$DNL_{cor}(k) = \frac{\Delta V(k+1) - \Delta V(k) - Q}{Q} - \delta; \qquad \delta = \frac{1}{2^N} \sum_{k=0}^{2^N-1} \frac{\Delta V(k+1) - \Delta V(k) - Q}{Q} \tag{3}$$

Uncertainty Analysis

The total uncertainty of the proposed method is given by the uncertainty $u(T(k))$ of determination of transition code level $T(k)$ (2). Error sources and uncertainties influencing the accuracy of measurement are:

- Errors and uncertainties of reference voltage VDC that include errors and uncertainties of DC source and DC voltmeter and offset of the comparator
- The nonlinearity of dithering voltage covering its quantisation noise and nonlinearity of D-DAC
- The uncertainty of finite record $p_k(i)$ in (2) given by the statistical uncertainty and uncertainty of dithering amplitude W
- Errors caused by dynamic properties of the voltage comparator CMP. The overdrive dispersion and the dynamic errors of CMP can be suppressed by a convenient time shift Δt of strobe pulse (Fig. 1) synchronization of D-DAC and DAC UT.

Because of their different origin, we can assume that these sources are statistically independent. Most of them contain a bias component: offset of the comparator, accuracy of DC voltmeter. These bias components are removed from test results by applying the terminal definition. Moreover, using the same record for determination of results for a few adjacent transition code levels covered by $2W$, e.g., for DNL estimation suppresses these bias errors also.

The uncertainty of the DC voltmeter consists of the uncertainty given by a voltmeter vendor and intrusion of superimposed dithering signal on the measured DC voltage. The incoherency between the DC voltmeter measuring time and the dithering period causes a voltage shift of

the measured DC value. Let suppose that the integration time of the DC voltmeter covers (J+ε) periods of the dithering signal, where *J* is an integer number and ε is a decimal remainder in the range -0.5≤ ε <0.5. Then the maximal value of the uncertainty component caused by this effect is 0.5W/(*J*+0.5). Let suppose, Then the uncertainty $u_q(V_{DITH})$ of dithering voltage V_{DITH} at the output of D-DAC is:

$$u_q(V_{DITH}) = a \cdot \left(\frac{2W_{D-DAC}}{2^b - 1}(c+1) \right) \tag{4}$$

The constant b represents the resolution of D-DAC with the maximal *DNL*=c [LSB]. The combined uncertainty of measurement results from equation (2) is:

$$u^2(T(k)) = u^2(V_{DC}) + u^2(\Delta V(k)) \tag{5}$$

The first component covers the above analyzed effects. The second component in (6) expresses uncertainty consisting of uncertainty of dithering amplitude u(*W*)=*a*.*u*(WD-DAC) and statistical uncertainty given by processing of finite record of pk(i) - u(pk(i)):

$$u^2(\Delta V(k)) = u^2(W)\left(\frac{1}{M}\sum_{i=1}^{M} p_k(i) \right)^2 + \frac{W^2}{M^2}\sum_{i=1}^{M} u^2(p_k(i)) = u^2(W) + u^2(pk) \tag{6}$$

The second component - $u(p_k(i))$ is given by the uncertainty of values in the transformed array $p_k(i)$, where the elements in the recorded array have binomial distribution. The maximum dispersion of the second component (2) σ^2 = 0.25 M, and the total uncertainty in the worst case is:

$$u^2(p(k)) = \frac{W^2}{M} 0.25 \tag{7}$$

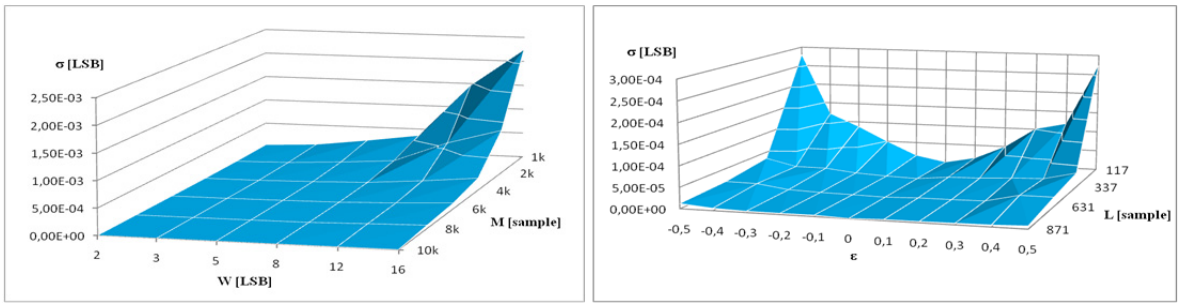
Dithering voltage covers only a few LSBs of DAC UT, and therefore uncertainty of its amplitude u(W) is relatively very small in comparison with the total uncertainty of determination of *T*(*k*) and could be neglected.

3. Experimental Results

The simulation of the combined dependence of the uncertainty on record length *M* as well as on amplitude of dithering *W* is shown on Fig.2.a.). Simulation results confirm the theoretical analysis, that the most important uncertainty factor is the number of samples and influence of dithering amplitude *W*.

The effect of the incoherency on the final uncertainty of measurement is shown in Fig. 2.b.). The number of samples in record *M* is constant and equals to 10000, and the number of period of dithering voltage *L* was chosen to be relatively prime. Error of coherency ε from interval [-0.5,0.5] was added to *L*. The strict coherency is required only for a small number of dithering signal periods *L*. The influence of coherence error ε quickly decreases with the increase of the number of periods of dithering.

Experimental validation was performed using the 14 bits DAC UT AD7534T by Analog Devices. Because of the high accuracy of the tested DAC, a chosen number of the most significant bits (8 or 10 bits mode) was used to generate DAC UT basic sawtooth signal. The rest of the least significant bits were used to insert additional known nonlinearity representing the 0,25 LSB of the tested resolution. The DNL_n characteristics of the DAC UT measured by the new proposed method were compared with reference DNL_s obtained from the static testing procedure. The standard deviations σ of deviation of DNL measured by static and proposed method $\sigma(\Delta DNL(k)) = \sigma(\Delta(DNL_s(k)) - DNL_n(k)))$ are shown in Table 1 for both DAC UT modes.



(a) (b)

Fig. 2. Dependence of standard deviation of difference between INL characteristics on amplitude of dithering W and different record length M at constant ratio M/L=11.48.

Record length	σ (Δ*DNL*(*k*)) - 8 bit	σ (Δ*DNL*(*k*)) – 10 bit		Dithering voltage amp.	σ (Δ*DNL*(*k*))
$M=10^4$	0.0215 LSB	0.0415 LSB		W = 2 LSB	0.0290 LSB
$M=10^5$	0.0125 LSB	0.0283 LSB		W = 5 LSB	0.0272 LSB
$M=5.10^5$	0.0102 LSB	0.0251 LSB		W = 8 LSB	0.0327 LSB

Table 1. Measured standard deviations ΔDNL characteristics measured as functionby of record length M for superimposed errors 0,25 LSB and amplitude of the dithering voltage for 8/bit and 10 bit mode of the DAC UT.

4. Conclusion

In the paper, a new method for DAC testing under dynamic conditions was analysed. A detailed description of the test setup followed by mathematical models and uncertainty analysis is presented. The new proposed method was validated both by simulations and experiment on real setup under different working conditions. The results were compared with the results obtained from the standard static test method. The juxtaposition showed that the results achieved by this method are quite similar to the results obtained by the standardized static test method.

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